Code: AE27 **Subject: DIGITAL HARDWARE DESIGN**
Time: 3 Hours **Max. Marks: 100**

DECEMBER 2007

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 A Choose the correct or best alternative in the following: (2x10=20)

a. With respect to package body in VHDL which of the following is true-

(A) Package body is always associated with a package declaration.
(B) A package declaration can have at most one package body associated with it.
(C) Name of the package body must be same as that of the package declaration with which it is associated.
(D) All of the above.

b. If AB' +A'B=C then AC'+A'C =

(A) C **(B)** B
(C) 0 **(D)** 1

c. Product of sum expression for $f(w,x,y,z) = \prod (0,1,2,3,4,7,8,11,12,13,14,15)$ will yield result

(A) (Y+Z)(Y'+Z')(W+X)(W'+X') **(B)** (Y+Z')(Y'+Z)(W'+X)(W+X')
(C) (Y+Z)(W+X)(W'+X') **(D)** None of the above

d. A switching function whose true vertices can be separated by a linear equation from its false ones is called _____.

(A) Threshold function **(B)** Linearly separable function
(C) Random function **(D)** Excitation function

e. The number of flip-flops required to build a binary counter to count from 0 to 1024 is

(A) 12 **(B)** 10
(C) 20 **(D)** 8

f. The programmable modules are advantageous for the reasons listed as

(A) Cost of IC does not depend on the number of pins but on the number of gates included in the chip.
(B) Use of programmable module does not allow modification.
(C) Cost of IC depends on the cost of designing the chip.
(D) Cost depends on the number of chips of same kind being produced.

g. A set of micro instructions for control of a computation sequence is called_____

(A) Micro-program **(B)** Macro-program
(C) Sub-program **(D)** None

h. Most typical use of counter is

(A) To generate timing signal.
(B) Generate clock of different frequencies.
(C) Both **(A)** and **(B).**
(D) None.

B **State TRUE or FALSE**

i. A faster alternative to ripple carry adder can be obtained at the cost of more gates with larger number of inputs.

(A) TRUE **(B)** FALSE

j. Multiplexer tree is large multilevel multiplexer network with fewer inputs.

(A) TRUE **(B)** FALSE

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Simplify the following expressions using K-map also represent them through basic gates

(i) $f(A,B,C,D,E) = \sum(2,3,6,10,12,13,14,16,18,22,26,28,29,30)$

(ii) $f(A,B,C,D,E) = \prod(1,3,4,5,9,14,15)$ d (2,6,11) **(8)**

b. List the major capabilities provided by VHDL. **(4)**

c. List the limitations of two level networks. **(4)**

Q.3 a. What do you mean by combinational and sequential circuits? What are synchronous and asynchronous circuits? **(4)**

b. What are the limitations of a gated latch for using them in a synchronous network? **(4)**

c. Reduce the expression using tabular method and implement the circuit using basic logic gates

$f2(A,B,C,D) = \prod(0,2,3,6,7,8,9,10,13)$ **(4)**

d. Obtain decomposition for the function

$f(w,x,y,z) = w'x'z'+wx'z+w'yz+wyz'$ **(4)**

Q.4 a. For the binary cell define the following timing parameters

(i) Setup (ii) Pulse width

(iii) Hold time (iv) Propogation delay **(4)**

b. Design a synchronous counter with JK flip-flop and basic gates to count 000,111,101,110,001,010,000 **(8)**

c. What do you understand by explicit and implicit sequencing of microinstructions? **(4)**

Q.5 a. How are ROM modules classified as per the setting of their contents? **(4)**

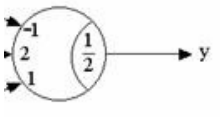
b. Differentiate between:

(i) PLA's & ROMs

(ii) Priority and binary decodes **(4)**

c. For the given switching function

$f(x_1, x_2, x_3, x_4) = \sum(2, 3, 6, 7, 10, 12, 14, 15)$ Find minimal threshold logic realization **(4)**



d. Find the function $f(x_1, x_2, x_3)$ realized by the threshold network shown in Fig.1. **(4)**

Fig.1

Q.6 a. List the components of the RTL data subsystem. Explain each component in brief. **(8)**

b. Write VHDL code entity for 2X4 decoder by using any two type of modeling-
(i) structural style (ii) Data flow style
(iii) Behavioral style of modeling **(6)**

c. Implement full adder module using multilevel implementation with XOR & NAND gates. **(2)**

Q.7 a. State the various advantages and disadvantages of programmable modules. **(6)**

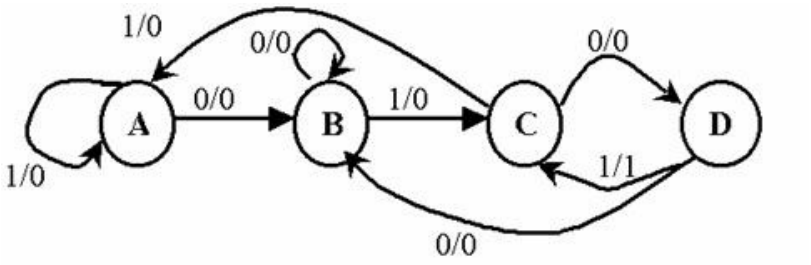
b. Define Mealy and Moore machine. **(2)**

c. Find a state assignment for the following machine which reduces the inter-dependency of the state-variables. **(8)**

PS (Present State)	NS (Next State)	
	X=0	X=1
A	E	B
B	E	A
C	D	A
D	C	F
E	F	C
F	E	C

Q.8 a. Illustrate the basic concept of microprogramming. What do you understand by the term 'Horizontal microprogramming' and 'Vertical microprogramming'. **(8)**

b. Design a sequential network using D-flip-flops for a system which has the following state diagram **(6)**



c. Specify which of the arrays is programmable and which is fixed in a PROM, PAL and FPLA. **(2)**

Q.9 a. What do you understand by hazards in switching circuits? What are dynamic hazards? **(4)**

b. Write a mixed style VHDL code for the one-bit full adder using two X-OR three AND & one OR gate. **(8)**

c. Write a VHDL code for a 4-bit shift-register in behavioural style of modelling. **(4)**