Code: A-27 **Subject: DIGITAL HARDWARE DESIGN**

Time: 3 Hours **June 2006** **Max. Marks: 100**

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: (2x10)

a. Hamming code for LED-SEC has the following code received: 0110110. The corrected code is

(A) 0010110 **(B)** 0010110
(C) 1110110 **(D)** 0111110

b. K-map for a switching function is shown below:

YZ \ WX				
	1			1
	1	1	1	1
		1	1	
	1			1

Identify which one of the following is true. The function has

(A) One essential and two non-essential prime implicants.
(B) Two essential and one non-essential prime implicants.
(C) Two essential and two non-essential prime implicants.
(D) Three essential prime implicants only.

c. In an FPLA

(A) Only AND arrays are programmable.
(B) Only OR arrays are programmable.
(C) Both the AND array and the OR array are programmable.
(D) None of these are programmable.

d. Simplifying the following Boolean function $Y(A, B, C, D) = \pi M(1, 5, 7, 8, 9, 10, 11, 12, 13, 14, 15)$ gives

(A) $\overline{A}(\overline{B}+\overline{D})(C+\overline{D})$ **(B)** $A(\overline{B}+\overline{D})(\overline{C}+D)$
(C) $\overline{A}(\overline{B}+D)(\overline{C}+D)$ **(D)** $\overline{A}(\overline{B}+\overline{D})(\overline{C}+\overline{D})$

e. A function $f(x_3, x_2, x_1, x_0)$ is described by the expression $z = x_3(x_1 + x_2x_0)$. Applying Shannon's decomposition with respect to x_0, we get

(A) $z = (x_3\, x_1)x_0' + x_3(x_2 + x_3)x_0$

(B) $z = (x_3\, x_1)x_0' + x_3(x_1 + x_2)x_0$

(C) $z = (x_2\, x_1)x_0' + x_2(x_3 + x_1)x_0$

(D) $z = (x_2\, x_3)x_0' + x_3(x_2 + x_3)x_0$

f. For a Moore canonical network, the input and output networks have a propagation delay of 2.5 ns and 3 ns respectively. The set up time of the register cells is 0.3 ns and the propagation delay is 1 ns. The network input stabilises no later than 2 ns after the triggering edge of the clock. The output needs to be stable for 3 ns before the next triggering edge. The maximum clock frequency for the above network approximately is

(A) 100 MHz **(B)** 120 MHz
(C) 50 MHz **(D)** 140 MHz

g. Identify one expression, which is not the characteristic expression of any flip-flop.
(A) Q (t+1) = D (t) **(B)** Q (t+1)= Q(t) R^1(t) + S(t)
(C) Q (t+1) = Q(t) K^1(t)+Q^1(t) J(t) **(D)** Q (t+1)= Q(t) +T(t)

h. In VHDL, a configuration is needed to
(A) Bind architecture body to its entity declaration.
(B) Bind a component with an entity.
(C) Specify a top-level entity in terms of low level entities.
(D) All of the above.

i. The U and Z values in model simulation refer to
(A) User defined and high impedance values.
(B) Undefined and high impedance values.
(C) U and z formats.
(D) User and z models.

j. A postponed process means
(A) a process that executes only at the end of all deltas of the simulation time in which an event triggered the process to resume execution.
(B) A process that is postponed before a trigger process is initiated.
(C) A process that is postponed till the next process execution starts.
(D) A keyword for postponing the existing process.

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Use the tabulation procedure to generate the set of prime implicants and to obtain all minimal expressions for the following function.

$$f(w,x,y,z)=\sum(0,1,4,5,6,7,9,11,15)+\sum_{\phi}(10,14)$$

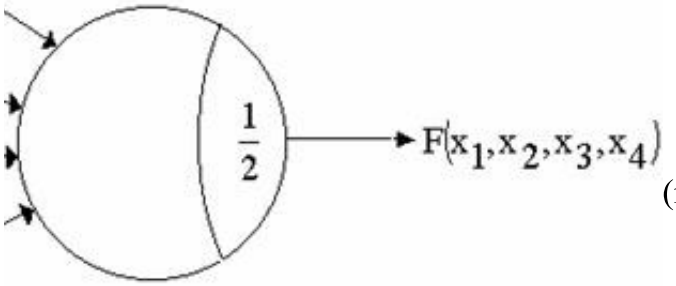
(7)

b. Construct the decomposition chart for the function given below:

$$f(w,x,y,z)=\sum(1,3,5,7,8,11,13,15)$$

Indicate all possible decompositions and determine specifically the functions F and ϕ such that $f(w,x,y,z)=F[\phi(x,y),w,z]$ **(4)**

c. Find the function of $f(x_1,x_2,x_3,x_4)$ realised by each of the threshold network shown in the following figure. Show the map of each function. **(5)**



(i) Priority encoder (ii) Shift register (iii)

b. Determine a ROM and a PLA based implementation for the following system.

Input : $\underline{a} = (a_2, a_1, a_0), a_j \in (0,1)$

$\underline{b} = (b_2, b_1, b_0), b_j \in (0,1)$

Output: $z = (z_1, z_0), z_j \in (0,1)$

Function:
$$z = \begin{cases} 1 \text{ if } a = (b-1) \bmod 8. \\ 2 \text{ if } a = b \\ 0 \text{ otherwise} \end{cases}$$

Where a, b, z are the integers represented by the corresponding vectors in radix-2 number system. Note that –1 mod 8 is defined as 7. **(8)**

Q.4 a. Define pulse mode and fundamental mode in FSM. **(5)**

b. Design a sequential system with one binary input x and one binary output z. The output at time t is 1 whenever x(t-3, t) = 0101. Write the state table and draw the state diagram. **(4)**

c. For the following machine shown in Table 1, find the equivalence partition and a corresponding reduced machine in standard form. **(7)**

PS	**NS, Z**	
	x = 0	**x =1**
A	D, 0	H, 1
B	F, 1	C, 1
C	D, 0	F, 1
D	C, 0	E, 1
E	C, 1	D, 1
F	D, 1	D,1
G	D, 1	C,1
H	B, 1	A,1

Table 1

Q.5 a. For the incompletely specified machine shown below in Table 2, find a minimum state reduced machine containing the original one. **(10)**

PS	NS, Z		
	I_1	I_2	I_3
A	C,0	E,1	-
B	C,0	E,-	-
C	B, -	C,0	A,-
D	B, 0	C,-	E,-
E	-	E, 0	A,-

Table 2

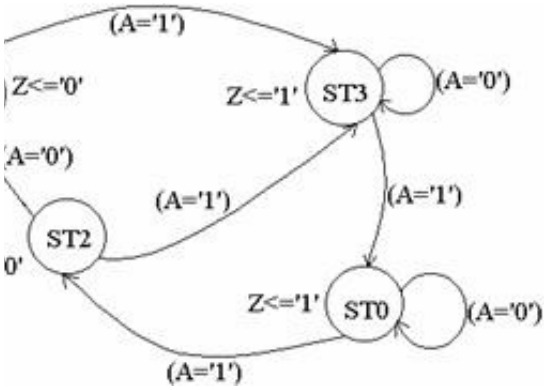
b. Distinguish between Mealy and Moore machines. **(6)**

Q.6 a. Generate an ASM chart for adding two unsigned 8-digit BCD numbers using array variables. **(6)**

b. Compare PROM, PAL and FPLA devices. **(4)**

c. Two 4 bit registers X and Y are loaded with values. On a start signal, X and Y are compared. If X>Y, flip flop A is set to 1. If X<Y, a flip flop B is set to 1. If X = Y, flip flop E is set to 1. It is needed to load X and Y and clear all flipflops and give a start signal. On start, the MSBs of X and Y (namely X_3 and Y_3) are compared. Write a ASM chart, state transition diagram and operations that take place during a clock interval. **(6)**

Q.7 a. A state transition diagram for a Moore finite state machine is shown below:



Write the behaviour model to implement the above, using a single process and case statement. **(8)**

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b. Write the VHDL code for the following:

(i) 4:1 multiplexer.

(ii) D-Latch. **(8)**

Q.8 a. Determine which of the following functions is symmetric and identify its a-numbers and variables of symmetry.

(i) $f(x_1, x_2, x_3, x_4, x_5) = \sum (0, 3, 5, 6, 10, 12, 15, 18, 20, 23, 25, 30)$

(ii) $f(x_1, x_2, x_3) = \sum (0, 2, 3, 4, 5, 7)$

(iii) $f(x_1, x_2, x_3, x_4) = \sum (0,5,6,9,10,15)$ **(10)**

b. Write a note on computer aided design tools which you have studied. **(6)**

Q.9 a. Write explanatory notes on (Any **FOUR**)

(i) FPGA

(ii) Microinstruction sequencer.

(iii) Dataflow and structural style modelling in VHDL.

(iv) Hazards and races in ASM.

(v) Incompletely specified machines. **(4 x 4 = 16)**