Code: A-27 **Subject: DIGITAL HARDWARE DESIGN**
Time: 3 Hours **Max. Marks: 100**

NOTE: There are 11 Questions in all.

- **Question 1 is compulsory and carries 16 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Answer any THREE Questions each from Part I and Part II. Each of these questions carries 14 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: (2x8)

a. In a strongly connected machine

(A) every state has same output
(B) all states are compatible
(C) every state is reachable from all states
(D) there exists a terminal state

b. Which of the following functions is symmetric function

(A) $x'y'z + xy'z' + x'yz'$. **(B)** $x'y'z + xy'z'$.
(C) $x'y'z + xyz'$. **(D)** $x'y'z' + x'yz' + xy'z'$.

c. In an 8-bit ring counter the preloaded pattern repeats after

(A) 8 clock pulses. **(B)** 16 clock pulses.
(C) 4 clock pulses. **(D)** 6 clock pulses.

d. The frequency of the clock generated by the statement "clk ⇐ not clk after 10 ns"; is

(A) 50 MHz. **(B)** 5 MHz.
(C) 500 MHz. **(D)** 33 MHz.

e. For the merger graph shown in the compatible state pairs are

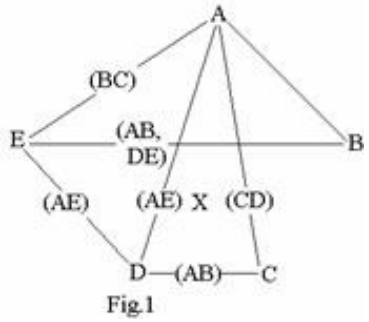

Fig.1

(A) (AB); (AC); (CD)
(B) (ABC); (CD)
(C) (AD); (AB); (AC)
(D) (ABCDE)

f. The ASM chart shown in Fig.2 represents

(A) MOD-2 counter
(B) MOD-3 counter
(C) MOD-4 counter
(D) MOD-5 counter

g. Time delay in an FPLA is

(A) more as compared to PAL **(B)** less as cc
(C) equal to PAL **(D)** zero

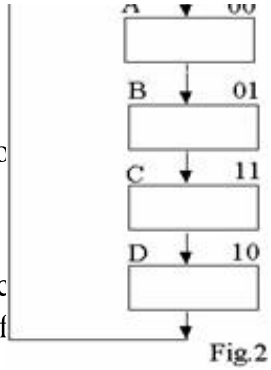

Fig.2

h. $F = \overline{B}D + \overline{A}B\overline{C} + A\overline{C}D + \overline{A}BC$ represents the switc one of the following expression represents the complementary function of

(A) $\overline{B}\overline{D} + A(\overline{D} + B\overline{C})$. **(B)** $AB + \overline{B}D + C\overline{D}$.
(C) $\overline{A}\overline{B} + B\overline{C} + \overline{C}D$. **(D)** $AB + \overline{B}C + \overline{C}\overline{D}$.

PART I
Answer any THREE Questions. Each question carries 14 marks.

Q.2 a. Determine
(i) canonical sum-of-products form for $f(x, y, z) = x'y + z' + xyz$.
(ii) canonical products-of-sums form for $f(x, y, z) = x'(y' + z)$. **(4)**

b. What do you understand by functionally complete operation? Prove that NAND and NOR operations are functionally complete. **(4)**

c. For the function $f(w, x, y, z) = \sum (0, 1, 2, 3, 4, 6, 7, 8, 9, 11, 15)$ find all prime implicants and indicate which are essential. Find a minimal expression for f. **(6)**

Q.3 a. Design a code converter which converts a BCD message into Excess-3 code. Realize this code converter using an appropriate ROM. **(8)**

b. Draw the output logic macro cell (OLMC) of a GAL and explain its function. **(6)**

Q.4 a. Design a mod-8 counter which counts in gray code. Realize it using D flip-flop. **(6)**

b. A synchronous sequential circuit has two JK flip-flops A and B with positive edge clock inputs, two input variables x and y and one output variable z. The flipflop input functions and circuit output function are given as $J_A = Bx + \overline{B}\overline{y}$, $K_A = \overline{B}x\overline{y}$, $J_B = \overline{A}x$, $K_B = A + x\overline{y}$, $z = Axy + B\overline{x}\overline{y}$. For the synchronous sequential circuit described
(i) draw logic diagram.
(ii) derive next state equations for A and B.
(iii) construct state table. **(8)**

Q.5 a. Write behavioural VHDL code for 4-bit comparator with 6 bit output Y[0:5] where bits 0 to 5 represent equality, in-equality, greater than, less than, greater than or equal and less than or equal outputs respectively. **(7)**

b. Design 4:16 decoder using 2:4 decoder with structural VHDL modelling. **(7)**

Q.6 a. For the circuit shown in Fig.3 construct transition table and determine all critical and non critical races. Explore the possibility of cycles. **(10)**

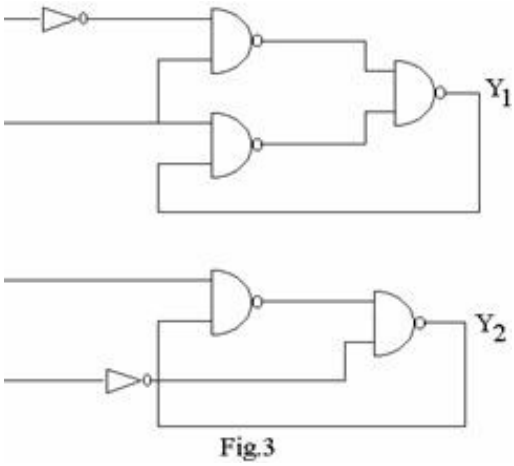

Fig.3

b. Draw the portion of an ASM chart starting from an initial state. There are two control signals x and y. If xy=10, register R is incremented by one and control goes to a second state. If xy = 01, R is cleared to zero and control goes from initial state to a third state otherwise control stays in the initial state. **(4)**

PART II

Answer any THREE Questions. Each question carries 14 marks.

Q.7 a. Find the reduced state table for the machine given below: **(9)**

PS	NS, Z_1Z_2			
	00	01	11	10
A	A, 00	E, 01	-, -	A, 01
B	-, -	C, 10	B, 00	D, 11
C	A, 00	C, 10	-, -	-, -
D	A, 00	-, -	-, -	D, 11
E	-, -	E, 01	F, 00	-, -
F	-, -	G, 10	F, 00	G, 11
G	A, 00	-, -	-, -	G, 11

b. Define fundamental mode and pulse mode of operations for a sequential machine. **(5)**

Q.8 a. Give a simple state assignment by choosing self dependent subset and utilizing partition with substitution theory for the machine given below: **(9)**

PS	NS		Z
	x=0	x=1	
A	D	C	1

B	A	D	0
C	B	E	0
D	E	B	0
E	F	C	0
F	C	D	0

b. The sequential machine shown below has a closed partition $\pi = \{\overline{A, C, D, F}\ ;\ \overline{BEG}\}$. Can you find another closed partition so that a parallel decomposition of the said machine is possible? **(5)**

PS	NS	
	x=0	x=1
A	F, 1	C, 0
B	E, 0	B, 1
C	D, 0	C, 0
D	F, 1	C, 1
E	G, 0	B, 0
F	A, 1	F, 1
G	E, 1	G, 0

Q.9 a. Design a two bit up down counter and show its implementation using an appropriate PAL. **(4)**

b. A system, consisting of two registers R_1 and R_2 and a flip flop E, counts the number of 1's loaded into R_1 and sets R_2 to that number. Draw the ASM chart for the system and design the control circuit using multiplexers. **(10)**

Q.10 a. A sequential network examines a group of 4 consecutive inputs and produces an output z =1 if input sequence 0101 or 1001 occurs. The network resets after every four inputs. Draw a Mealy state graph for the network and write state table and reduce it. **(8)**

b. Write VHDL code for 3-bit odd parity generator using dataflow description. **(6)**

Q.11 Write short notes on any **TWO** of the following:

(i) Digital design using CAD tools.
(ii) Vertical and horizontal microprogramming.
(iii) FPGA.
(iv) Equivalence between Mealy and Moore Machines. **(2 x 7 = 14)**