AMIETE – ET (OLD SCHEME)

Code: AE27 **Subject: DIGITAL HARDWARE DESIGN**
Time: 3 Hours **Max. Marks: 100**

JUNE 2010

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions, answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. In a four variable Karnaugh map eight adjacent cells give a

(A) Two variable term **(B)** single variable term
(C) Three variable term **(D)** four variable term

b. Why do we need additional SOP terms when programming an array logic cell?

(A) To improve dynamic timings
(B) To improve static timings
(C) To remove only static hazards
(D) To remove both static hazards and static glitches

c. Two's complement of a two's complement will return

(A) 0 **(B)** Same number with negative sign.
(C) Original number **(D)** None

d. Calculate the delay at an i-th stage in finding CY_i assuming that each stage of FA takes propagation time t_S

(A) 2 . t_S **(B)** 2 .i . t_S
(C) 2 / t_S **(D)** i. t_S

e. Race-around condition is associated with the _____.

(A) RS Flip Flop **(B)** JK Flip Flop
(C) MS-JK Flip Flop **(D)** D Flip Flop

f. How does a latch differ from a Flip Flop

(A) Output changes **(B)** Clock edge input
(C) Both **(A)** and **(B)** **(D)** None

g. In VHDL, Configuration statement is used to

(A) bind the entity and the architecture
(B) bind the components and the functions
(C) bind the package and the Libraries
(D) bind the component instance to an entity-architecture pair

h. The entity specifies

(A) the number of ports **(B)** the direction of ports
(C) the type of ports **(D)** all the above

i. The mechanism for delaying the new value is called

(A) Statement concurrency **(B)** Event scheduling
(C) Both **(A)** and **(B)** **(D)** None of the above

j. All the statements enclosed by the PROCESS are

(A) Concurrent statements **(B)** Sequential statements
(C) Configuration statements **(D)** None of the above

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain how CAD software tools help to improve the productivity, correctness and quality of design. **(8)**

b. Realize XOR gates using AND, NOT and OR gate. **(4)**
c. Realize 4 bit adder circuit using 1-bit adder. **(4)**

Q.3 a. Explain the working of clocked SR Flip Flop with circuit diagram. **(5)**
b. Explain the CLOCK SKEW with timing diagrams. **(7)**

c. Realize positive edge-triggered D-type Flip Flop connected as divide-by-2 counter. **(4)**

Q.4 a. Draw the circuit of binary-to-octal converter using decoders. **(6)**

b. Draw the 1 to 8 demultiplexer circuit with truth table. **(6)**

c. Design a 4 bit ripple counter (Asynchronous) circuit using JK Flip Flop. **(4)**

Q.5 a. Design a digital circuit for the pulse-train generator that generates a sequence of N pulses each time it is triggered by a positive transition at its START input. The value of N may vary from 0 to 7. **(8)**

b. Design a 4-bit shift register using D Flip Flop. **(4)**

c. Design a 4 bit PISO circuit using D Flip Flop. **(4)**

Q.6 a. Design a sequence recognizer for detecting the sequence 1001. **(10)**

b. Explain all the design constructs of VHDL with syntax. **(6)**

Q.7 a. Write a VHDL code to describe D-Latch with clock enabled. **(4)**

b. Write a VHDL code for the 2-bit up-counter with synchronous reset. **(6)**

c. Write a VHDL code for a Priority Encoder. **(6)**

Q.8 a. With the aid of a Quine-McCluskey (tabular) method derive minimal sum of products expressions for the following: **(8)**

$$f(X_1, X_2, X_3, X_4) = \sum (0,1,2,5,6,7,8,9,10,13,15)$$

b. Decompose the following functions **(8)**

$F(G(X_1, X_2), X_3, X_4)$ and $F(G(X_1, X_3), X_2, X_4)$

Q.9 a. Realize 13 variable symmetric function using 10 full adders and 1 decoder. **(8)**

b. Write the procedure for identifying symmetric functions. **(8)**