BT-5/D09

COMPUTER HARDWARE DESIGN

Paper : ECE -303 (E)

Time : Three Hours] **[Maximum Marks : 100**

Note : Attempt any *five* questions.

1. (a) Explain in brief different instruction types that can be used in a computer. 5
   (b) Explain in detail the concept of parameter passing with the help of an example. 8
   (c) Explain with the help of an example all the valid addressing modes that can be used by the user. 7
2. Consider a computer that has a number of registers such that the three registers R0 = 2000, R1 = 3500 and R2 = 2000. Show the effective address of memory and the registers' contents in each of the following instructions (assume that all numbers are decimal) :
   (a) MOVE 700(R0), R2
   (b) STORE R0, 300 (R2)
   (c) ADD (R0) +, R2
   (d) LOAD #7000, R2
   (e) SUBTRACT – (R1), R2. 20
3. (a) Design a BCD adder using a 4-bit binary adder and the least number of logic gates. The adder should receive two 4-bit numbers A and B and should produce 4-bit sum and a carry output. 15
   (b) Explain in detail the concept of parameter passing with the help of an example. 5
4. (a) What is the average access time of a system having three levels of memory, a cache, memory, a semiconductor main memory, and a magnetic disk secondary memory, if the access times of the memories are 20 ns, 100 ns and 1 ms, respectively. The cache hit ratio is 90% and the main memory hit ratio is 95%. 15
   (b) Explain in detail, the structure of a Multiplier control unit with the help of a block diagram. 5
5. Design a 16-bit sliced ALU using four copies of the AMD 2901 4-bit slice. Use a carry lookahead and use NAND gates to design the necessary carry-generator logic. Give a block diagram of your design and give a set of Boolean equations that specify the carry lookahead equation. 20
6. (a) Explain with the help of a block diagram a 1-D RAM addressing scheme. 10
   (b) Explain the differnt forms of parallel processing classification of parallel structures in detail. 10
7. (a) Define pipelining in a system. Explain the structure of an *m*-stage pipeline, and draw a block diagram to illustrate a 2-stage pipelined microprogram control unit. 10
   (b) Prove informally the following general property of a single function pipeline. If K is the maximum number of X's in any row of the pipeline's reservation table, then $K < L_{min}$, the minimum average latency. 10
8. Explain in detail the following :
   (a) Magnetic Tape Memories.
   (b) Tree Networks.
   (c) Array Processors.
   (d) Crossbar Networks. $5 \times 4 = 20$

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