Code: AC07 / AT07 **Subject: COMPUTER ARCHITECTURE**
Time: 3 Hours **Max. Marks: 100**

DECEMBER 2010

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after half an hour of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 **Choose the correct or the best alternative in the following:** (2×10)

a. 'Cycle Stealing' is associated with

   (A) Data transfer among registers **(B)** DMA
   (C) Pipelining **(D)** Microprogramming

b. Using an additional NOT gate, a JK flip-flop can be converted into

   (A) T flip-flop **(B)** RS flip-flop
   (C) Master Slave flip-flop **(D)** D flip-flop

c. A given memory chip has 16 address pins and 4 data pins. It has the following number of locations.

   (A) 2^4 **(B)** 2^{12}
   (C) 2^{48} **(D)** 2^{16}

d. Break points are used for

   (A) stopping a program at a desired place
   (B) manipulating the stack
   (C) executing each instruction individually
   (D) calling a subroutine

e. A truth table of n variables has _____ minterms.

   (A) n^2 **(B)** $(n-1)^2$
   (C) 2^n **(D)** 2^{n-1}

f. Dual of $a + b \bullet c$ is

   (A) $(a + b) \bullet (a + c)$ **(B)** $a \bullet (b + c)$
   (C) $a' \bullet (b' + c')$ **(D)** $(a' + b') \bullet (a' + c')$

g. The condition to detect overflow during the addition of two binary numbers is

(A) C_n XOR C_{n-1} (B) C_n NOR C_{n-1}

(C) C_n OR C_{n-1} (D) C_n AND C_{n-1}

h. A microprocessor has a data bus with 64 lines and an address bus with 32 lines. The maximum number of bits that can be stored in this memory is

(A) 32×2^{32} (B) 32×2^{64}

(C) 64×2^{32} (D) 64×2^{64}

i. Pipeline arithmetic units are used to implement

(A) Floating point operations
(B) Multiplication of fixed-point numbers
(C) Both (A) and (B)
(D) None of the above

j. Which memory is faster?

(A) Register   (B) Cache
(C) RAM   (D) Hard disk

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Draw the logic diagram of a 2-to-4 line decoder with NAND gates. Give its truth table also. **(6)**

b. Draw a block diagram to illustrate the basic organization of computer system and explain the function of various units. **(6)**

c. Explain the working of a JK Flip Flop. **(4)**

Q.3 a. Register A holds the 8-bits 11011001. Determine the B operand and the logic micro operation to be performed in order to change the value in A to: **(6)**
(i) 01101101   (ii) 11111101

b. Specify the IEEE proposed floating point single format representation in hexadecimal for number: -38.5. **(4)**

c. Simplify the following Boolean function in POS form using K-maps
F (A, B, C, D) = $\sum$ (0, 2, 4, 5, 6, 8, 10, 13, 15)
Also draw a logic diagram using only NAND gates. **(6)**

Q.4 a. Explain the three different types of instruction code formats of a basic computer namely-memory reference, register-reference and I/O instruction. **(8)**

b. Explain the diagram and function of 4 bit adder-subtractor. **(8)**

Q.5 a. List the differences between a branch, a subroutine call and an interrupt. **(6)**

b. (i) How many 128×8 RAM chips are needed to provide a memory capacity of 2048 bytes?
(ii) How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips? **(5)**

c. Differentiate between SRAM and DRAM. **(5)**

Q.6 a. Explain the working of the instruction pipelining with the help of a diagram. **(8)**

b. An instruction is stored at location 500 with its address field at location 501. The address field has the value 300. A processor register Rl contains the number 100. Evaluate the effective address if the addressing mode of the instruction is **(8)**
(i) Direct
(ii) Relative
(iii) Register indirect
(iv) Index with R1 as lndex register
Make suitable assumptions if any.

Q.7 a. Write an assembly program to convert a 4digit BCD number to its binary equivalent. **(6)**

b. Briefly explain how zero-address instructions are evaluated in the basic computer. **(4)**

c. Describe Booth's algorithm for multiplication. **(6)**

Q.8 a. What is the need of a control unit in a computer? What is the difference between hardwired control and micro-program control? What are their advantages and disadvantages? **(8)**

b. Perform subtraction with the following unsigned binary numbers by taking the two's complement of the subtrahend. 11011 – 01101. **(8)**

Q.9 a. Write short note on cache memory. **(8)**

b. Briefly describe the working of DMA. **(8)**