AMIETE – CS/IT (OLD SCHEME)

Code: AC07 / AT07 **Subject: COMPUTER ARCHITECTURE**
Time: 3 Hours **Max. Marks: 100**

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2 □10)**

a. The 8 bit register AR, BR and CR contain the following values initially:
AR=00100011 BR=00100011 CR=00011101
After execution of following sequence of micro-operations
AR←AR–1
BR←BR+AR
CR←BR–CR
CR will contain

(A) 01101000 **(B)** 01101001
(C) 01101000 **(D)** 01001001

b. Which of the following is not a part of instruction cycle?

(A) Fetch phase **(B)** Decode phase
(C) Wait Phase **(D)** Execute phase

c. The following segment of instructions belong to
ADD R1
MOV R1, R2
MUL R3
OUT 03H

(A) General Register Organization CPU
(B) Accumulator Type CPU
(C) Stack Type CPU
(D) information not sufficient to decide

d. Which pair of values represents -51_{10} in 8 bit 2's complement and signed magnitude respectively?

(A) 11100101, 00011011 **(B)** 11100001, 10011011
(C) 11100101, 00011011 **(D)** 11001101, 10110011

e. While comparing static and dynamic RAM for the packing density (representing number of storage cells per unit area) feature, one finds

(A) it is same in both.
(B) it is more in case of static RAM
(C) it is more in case of dynamic RAM
(D) all the above are possible

f. Arrange the following memory in order of their increasing access time i.e. the memory with lowest access time first and the memory with highest access time last

(i) CPU registers (ii) RAM
(iii) Hard disk (iv) Cache Memory

(A) (i), (ii), (iii), (iv) **(B)** (iii), (i), (ii), (iv)
(C) (i), (iii), (iv), (ii) **(D)** (i), (iv), (ii), (iii)

g. The address to the next instruction lies in

(A) Program Counter **(B)** Instruction Register
(C) Memory Buffer Register **(D)** Accumulator register

h. A CPU has 20 bit address bus connected to a 16 bit wide memory through a data bus of same width. The total volume of addressable memory available to the CPU is

(A)  **(B)** 
(C)  **(D)** 8 mega byte

i. How many memory chips of  are needed to build a memory capacity of  ?

(A) 64 **(B)** 16
(C) 32 **(D)** none of these

j. Let A and B be the two Boolean variables with  representing complement of A. Then the Boolean expression A+  B is equivalent to

(A) A+B **(B)** AB
(C) A+BA **(D)** none of the above

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Solve the following Boolean function using Karnaugh map. **(4)**

$F(A,B,C,D)=\sum (0,1,4,5,8,11,13)$

b. Write a short note on virtual memory organization. **(8)**

c. Construct a 16-to-1-line multiplexer using two 8-to-1-line multiplexers and a 1: 2 line decoder. (Draw block diagram only). **(4)**

Q.3 a. Design a 8 bit bus system to read data from any of the four 8 bit registers A, B, C and D. Use appropriate number of selection lines and draw the function table. Show the block diagram making use of multiplexers. **(8)**

b. Identify the memory operation (read/ write) involved in following transfer statements . **(2)**

(i) R1 ← M[AR]

(ii) M[AR] ← R2

c. Draw a block diagram to represent the following conditional statement
if (P = 1) then (R2 ← R1) else if (Q=1) then (R3 ← R1). **(6)**

Q.4 a. Describe the concept of an instruction cycle. Explain the various phases involved in the instruction cycle. **(6)**

b. Describe the concept of interrupt I/O. Explain under what conditions the interrupt I/O is useful. Describe how the interrupt cycle is executed. **(6)**

c. Compute 81_{10}-119_{10} using 8 bit 2's complement arithmetic. **(4)**

Q.5 a. Write program segments in assembly language to evaluate the following arithmetic statement: **(10)**

X=(A*B)+ (C * D) + (E * F)
Assuming that the CPU given is of the type
(i) Single accumulator organization
(ii) Stack organization

b. What is an addressing mode? Describe following addressing modes with an example for each **(6)**

(i) Immediate addressing modes
(ii) Register addressing mode
(iii) Register indirect addressing mode

Q.6 a. Explain briefly how interrupts are handled. **(6)**

b. Describe the address sequencing in micro-programmed control unit with the help of suitable diagram. **(10)**

Q.7 a. Multiply 101111_2 with 111001_2 using Booth's algorithm where both numbers are positive. **(6)**

b. Explain how data transfer takes place using a DMA processor. Describe with the help of suitable block diagram. **(10)**

Q.8 a. A digital computer has a memory unit of 1M□16 and a cache memory of 4K words. The cache uses direct mapping with a block size of eight words. How many bits are there in the tag, index, block and word field of address format? How many blocks can the cache accommodate? Also show the cache organization. **(10)**

b. An address space is specified by 24 bits and the corresponding memory space by 16 bits. How many words are there in address space and how many in memory space? If a page contains 2K words, how many pages and blocks are there in the system? **(6)**

Q.9 a. Make a block diagram of associative memory and explain its working. **(8)**

b. With the help of a neat diagram explain how priority interrupts can be implemented using priority encoder. **(8)**