AMIETE – CS/IT (OLD SCHEME)

Code: AC07 / AT07 **JUNE 2009** **Subject: COMPUTER ARCHITECTURE**
Time: 3 Hours **Max. Marks: 100**

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2 ×10)

a. If a number represented in signed 2's complement form is 110011, then the decimal equivalent is

(A) $(-13)_{10}$. **(B)** $(-12)_{10}$.
(C) $(-19)_{10}$. **(D)** $(51)_{10}$.

b. Bubble input EX-NOR gate is equivalent to

(A) EX-NOR gate. **(B)** OR gate.
(C) AND gate. **(D)** NAND gate.

c. The equivalent POS representation of a Boolean function $y = \sum m(0,2,3,5) + d(7,9,12,15)$ is

(A) $\Pi M(0,2,3,5)$.
(B) $\Pi M(1,4,6) + d(7,9,12,15)$.
(C) $\Pi M(1,4,6,8,10,11,13,14)$.
(D) $\Pi M(1,4,6,8,10,11,13,14) \cdot d(7,9,12,15)$

d. A MUX is not used as a programmable device as

(A) It is a combinational circuit. **(B)** Do not have reduced logic.
(C) PROM is cheaper than MUX. **(D)** No feasible link is available.

e. In a clocked sequential circuit, input data must be remain at a constant value before the transition is called

(A) Set up time. **(B)** Pick up time.
(C) Hold time. **(D)** Settling time.

f. The characteristic table specifying the next state when input and present state is known is called

(A) Truth table. **(B)** State table.
(C) Excitation table. **(D)** Reduction table.

g. After fetching the instruction from the memory, the binary code of the instruction goes to

(A) Program counter. **(B)** Instruction register.
(C) Accumulator. **(D)** Instruction pointer.

h. In cycle stealing technique, allows the DMA controller to transfer

(A) Half of a data word at a time. **(B)** One block of data at a time.
(C) One data byte at a time. **(D)** One data word at a time.

i. Arithmetic shift right operation on $(-22)_{10}$ results

(A) $(1110101)_2$. **(B)** $(1101010)_2$.
(C) $(101010)_2$. **(D)** $(111011)_2$.

j. In direct mapping technique, if the main memory is of 64 K words and cache memory is of 1 K words, than there will be

(A) 6 tag bits & 9 index bits. **(B)** 10 index bits & 6 tag bits.
(C) 10 tag bits & 6 index bits. **(D)** 6 index bits & 9 tag bits.

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Design a sequential circuit, (with parallel load) whose function table is given below:- **(10)**

Clock	Load	Clear	Increment	Operation
↑	0	0	0	No change
↑	0	0	1	Increment the count by 1.
↑	1	0	×	Parallel load.
↑	×	1	×	Clear the o/p

Use JK Flip-Flop and design the circuit for three bits only.

b. What is excitation table? Give the excitation table for JK and SR flip-flop. **(2+2+2)**

Q.3 a. Discuss different methods used for re-presenting signed number. If we want to represent $(-18)_{10}$ in these methods, give the representation. Also state that how $(-18)_{10}$ can be represented in BCD. **(8)**

b. With help of common bus configuration, realise a hardware circuit to implement the register transfer statements of fetch cycle. **(8)**

Q.4 a. What is the significance of Branch & Save Return Address (BSA) instruction? Write the Micro-operation required to be performed when BSA instruction is executed. **(2+2)**

b. An register B has the control function for load, clear and increment operation are given below:-

$LD(B) = \bar{P}T_0 + PT_2 + \bar{Q}\bar{S}T_3$

$CLR(B) = \bar{P}T_1 + \bar{P}\,\bar{Q}T_3$

$INR(B) = \bar{S}T_3$

Where P,Q, S are control variables and $T_0, T_1, \ldots T_3$ are timing sequences. Draw the control gate circuitry for register B. **(6)**

c. Explain the function of Address register, Stack pointer Program counter and Accumulator. **(6)**

Q.5 a. State the classification of computer based on Instruction format. Write a, program to evaluate $x = \frac{P}{Q}(R + S - PQ)$ in each case. **(10)**

b. What is the advantage of Program interrupt? How it is to be implemented, in a computer system. **(6)**

Q.6 a. Design the microcode logic to generate the control signals for the relatively simple CPU having following:-

Instruction	**Instruction code**
AND B	1000 1000
OR B	1000 1001
XOR B	1000 1010
ADD B	1000 1100
SUB B	1000 1111

The above instructions have their usual meaning. **(8)**

b. Show the contents of the register E, A, Q & SC during the process of a division of $(10100011)_2$ by $(1011)_2$ using restoring algorithm. **(8)**

Q.7 a. Discuss the salient features of Asynchronous and Synchronous serial data transfer techniques. **(8)**

b. With neat block diagram discuss the working of content addressable memory unit. **(8)**

Q.8 a. A computer system has an associative cache. CPU accesses the following locations in the order shown:-
$[A, B, C, A, D, B, E, F, A, C, D, B, G, C_2, H, I, A, B]$
The cache memory consist of 8 words. The cache access time and main memory access time is 20 ns & 60 ns respectively. Calculate the hit ratio and its average access time. Assume FIFO replacement policy. **(8)**

b. Discuss page fault and page replacement policies of a virtual memory system. **(8)**

Q.9 Write short notes on the following (Any **TWO**):-
(i) FIFO Buffer.
(ii) Microprogram sequencer.
(iii) MicroInstruction formats. **($8 \times 2 = 16$)**