Code: AC07/AT07 **Subject: COMPUTER ARCHITECTURE**
Time: 3 Hours **Max. Marks: 100**

DECEMBER 2007

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: (2x10)

a. Dynamic RAM consumes _____ Power and _____ than the Static RAM.

(A) more, faster **(B)** more, slower
(C) less, slower **(D)** less, faster

b. The flag register content after execution of following program by 8085 microprocessor shall be

Program
SUB A
MVI B, $(01)_H$
DCR B
HLT

(A) $(54)_H$ **(B)** $(44)_H$
(C) $(45)_H$ **(D)** $(55)_H$

c. Which flag of the 8085's flag register is not accessible to programmer directly?

(A) Zero flag **(B)** Carry flag
(C) Auxiliary carry flag **(D)** Parity flag

d. Cache memory works on the Principle of

(A) Locality of data. **(B)** Locality of reference.
(C) Locality of memory **(D)** Locality of reference & memory.

e. Which of the following is a Pseudo instruction?

(A) SPHL **(B)** LXI
(C) NOP **(D)** END

f. A demultiplexer can be used as

(A) Encoder **(B)** Decoder.
(C) Multiplexer. **(D)** None of the above

g. Excess-3 equivalent representation of $(1234)_H$ is

(A) $(1237)_{Ex-3}$ **(B)** $(4567)_{Ex-3}$
(C) $(7993)_{Ex-3}$ **(D)** $(4663)_{Ex-3}$

h. Which of the memory holds the information when the Power Supply is switched off?

(A) Static RAM **(B)** Dynamic RAM
(C) EEROM **(D)** None of the above

i. Minimum no. of NAND gate required to implement a Ex-OR function is

(A) 2 **(B)** 3
(C) 4 **(D)** 5

j. Which of the following interrupt is maskable?

(A) INTR **(B)** RST 7.5
(C) TRAP **(D)** Both **(A)** and **(B)**

Answer any FIVE Questions out of EIGHT Questions.

Each question carries 16 marks.

Q.2 a. Explain direct mapping of cache memory system. **(7)**

b. What do you mean by locality of reference? **(3)**

c. A virtual memory system has an address space of 8K words, memory space of 4K words and Page & Block size of 1K words. The following page reference changes occur during a given time interval

4, 2, 0, 1, 2, 6, 1, 4, 0, 1, 0, 2, 3, 5, 7

Determine the four pages that are resident in main memory after each Page reference change if the replacement algorithm used is (i) FIFO

(ii) LRU. **(6)**

Q.3 a. With neat block diagram, explain how DMA controller is initialised for DMA data transfer. **(7)**

b. How data is transmitted in synchronous serial communication system? **(3)**

c. How many characters per second can be transmitted over a 1200 baud line in asynchronous serial transmission in following modes. Assume a character code is of eight bits.

(i) Synchronous Serial Transfer

(ii) Asynchronous Serial Transfer with 2 Stop bits.

(iii) Asynchronous Serial Transfer with one Stop bit. **(6)**

Q.4 a. A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part.

(i) How many bits are there in the operation code, the register code part and the address part?

(ii) Draw the instruction word format and indicate the number of bits in each part.

(iii) How many bits are there in the data and address inputs of the memory? **(9)**

b. What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand in to a processor register? **(7)**

Q.5 a. With neat flow chart discuss the procedure for floating point multiplication. Explain with the help of an example. **(10)**

b. Design a Three-bit array multiplier. Use AND gates and binary adders. **(6)**

Q.6 a. Write a Program to evaluate the arithmetic statement

$$P = \frac{(x - y + z) * (m * n - o)}{Q + R * S}$$

by using (i) Two address instructions

(ii) One address instructions

(iii) Zero address instructions. **(12)**

b. Convert the following arithmetic expression from infix notation to RPN.

A*B+B*(B*D+C*E). **(4)**

Q.7 a. With neat block diagram explain the function of a microprogram sequencer. **(6)**

b. What is subroutine? How is it executed by the processor? What is the importance of subroutine Parameters and data linkage? How is it established? **(10)**

Q.8 a. Design a 4-bit combinational incrementer and decrementer circuit. **(7)**

b. Show the hardware implementation of following statement.

$xy\,T_0 + T_1 + y'T_2 : AR \leftarrow AR + 1$.

where x, y are control functions and T_0, T_1, T_2 are T-states. **(7)**

c. Represent the given conditional control statement by two register transfer Statements with Control functions.

If (P = 1), Than $R_1 \leftarrow R_2$ else if (Q = 1) Than $R_1 \leftarrow R_3$. **(2)**

Q.9 a. Implement a 2-bit multiplier circuit by using Multiplexers. **(8)**

b. If $P = \sum(m_0, m_3, m_4, m_8, m_{12}, m_{13}, m_{15})$ and
$Q = \Pi(M_1, M_4, M_5, M_{12}, M_{14})$, Then find the expression for $X = P \oplus Q$ in SOP & POS.
(8)