Code: AC-07/AT-07 **Subject: COMPUTER ARCHITECTURE**

JUNE 2007

Time: 3 Hours **Max. Marks: 100**

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: **(2x10)**

a. The ASCII code for letter A is

(A) 1100011 **(B)** 1000001
(C) 1111111 **(D)** 0010011

b. The simplified expression of $\overline{(\overline{A+B})+\overline{C}}$ is

(A) $(A+B)C$ **(B)** $A(B+C)$
(C) $(C+A+B)$ **(D)** None of these

c. The negative numbers in the binary system can be represented by

(A) Sign magnitude **(B)** 1's complement
(C) 2's complement **(D)** All of the above

d. ABCD – seven segment decoder / driver in connected to an LED display. Which segments are illuminated for the input code DCBA = 0001.

(A) b, c **(B)** c, b
(C) a, b, c **(D)** a, b, c, d

e. How many flip-flops are required to produce a divide-by-32 device?

(A) 4 **(B)** 6
(C) 5 **(D)** 7

f. The content of a 4-bit register is initially 1101. The register is shifted 2 times to the right with the serial input being 101101. What is the content of the register after each shift?

(A) 1110, 0111 **(B)** 0001, 1000
(C) 1101, 1011 **(D)** 1001, 1001

g. How many different addresses are required by the memory that contain 16K words?

(A) 16,380 **(B)** 16,382
(C) 16,384 **(D)** 16,386

h. What is the bit storage capacity of a ROM with a 512' 4-organization?

(A) 2049 **(B)** 2048
(C) 2047 **(D)** 2046

i. DMA interface unit eliminates the need to use CPU registers to transfer data from

(A) MAR to MBR **(B)** MBR to MAR
(C) I/O units to memory **(D)** Memory to I/O units

j. How many 128×8 RAM chips are needed to provide a memory capacity of 2048 bytes?

(A) 8 **(B)** 16
(C) 24 **(D)** 32

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Design a sequential circuit with JK flip-flops to satisfy the following state equations:

$$A(t+1) = A'B'CD + A'B'C + ACD + AC'D'$$
$$B(t+1) = A'C + CD' + A'BC'$$
$$C(t+1) = B$$
$$D(t+1) = D'$$

(10)

b. Simplify the Boolean function F together with don't care condition

$$F(A,B,C,D) = \sum m(1,3,7,11,15) + d(0,2,5)$$

(6)

Q.3 a. Explain the Adder-Subtractor with the help of 2's complement. **(8)**

b. Design a combinational circuit using a ROM. The circuit accepts a 3-bit number and generates an output in binary number equal to the square of the input number.

(8)

Q.4 a. What is the result of executing an arithmetic shift left operation whose first input is –15 and whose second input is 3, when executed on a system that uses 8-bit two's complement integers? What

will be the result if the arithmetic shift right is used with second input = 3? **(8)**

b. Represent microinstructions for a microprogram of LD $r_1, (r_2)$ instruction at control memory addresses ^{a}j to $^{a}j+5$. How will the program counter increment for the next instruction? **(8)**

Q.5 a. Discuss various addressing modes in detail. Assert your answer with suitable examples. **(8)**

b. Evaluate the arithmetic statement $X = (A + B) * (C + D)$ using a general register computer with three address, two address and one address instruction format. **(8)**

Q.6 a. Write an assembly language program to convert a digital string into respective exactly opposite value. **(8)**

b. Explain Booth's multiplications algorithm through an example. Give an example of multiplicant and multiplier for which this algorithm takes the maximum time. **(8)**

Q.7 a. Using 8-bit 2's complement representation of negative numbers, perform the following computations:

(i) $-35 + (-11)$ (ii) $19 - (-4)$ **(8)**

b. Assume there are devices 0 to m-1 that have descending order of priorities 0 to m-1. Suppose interrupts are not grouped and occur in the order 5,7,1,4. The interrupts 7, 1 and 4 occur when the ISR5 was running. Processor architecture provides for in between ISR diversion to a higher priority interrupt. What will be the sequence of execution of the ISR instructions? **(8)**

Q.8 Consider a cache (M_1) and memory (M_2) hierarchy with the following characteristics:

M_1 : 16 K words, 50 ns access time

M_2 : 1 M words, 400 ns access time

Assume 8 words cache blocks and a set size of 256 words with set associative mapping.

(i) Show the mapping between M_2 and M_1.

(ii) Calculate the Effective Memory Access time with a cache hit ratio of $h = .95$. **(16)**

Q.9 Write short notes on the following:

(i) Direct Memory Access based data transfer.

(ii) Virtual memory.

(iii) Flip-Flops.

(iv) Multiplexer. **(4 × 4 =16)**