Code: C-07/T-07 **Subject: COMPUTER ARCHITECTURE**
Time: 3 Hours **June 2006** **Max. Marks: 100**

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: (2x10)

a. Which of the following expression is not equivalent to $\bar{x}$?

(A) x NAND x **(B)** x NOR x
(C) x NAND 1 **(D)** x NOR 1

b. Word 20 contains 40
Word 30 contains 50
Word 40 contains 60
Word 50 contains 70
Which of the following instructions does not, load 60 into the Accumulator

(A) Load immediate 60 **(B)** Load direct 30
(C) Load indirect 20 **(D)** both (A) & (C)

c. An interrupt for which hardware automatically transfers the program to a specific memory location is known as

(A) Software interrupt **(B)** Hardware interrupt
(C) Maskable interrupt **(D)** Vector interrupts

d. Synchronous means _____

(A) At irregular intervals **(B)** At same time
(C) At variable time **(D)** None of these

e. 'n' Flip flops will divide the clock frequency by a factor of

(A) n^2 **(B)** n
(C) 2^n **(D)** log(n)

f. In DMA the data transfer is controlled by

(A) Microprocessor **(B)** RAM
(C) Memory **(D)** I/O devices

g. The number of instructions needed to add n numbers and store the result in memory using only one address instructions is

(A) n **(B)** $n-1$
(C) $n+1$ **(D)** Independent of n

h. Negative numbers can not be represented in

(A) Signed magnitude form **(B)** 1's complement form
(C) 2's complement form **(D)** 8-4-2-1 code

i. Which of the following architecture is/are not suitable for realizing SIMD

(A) Vector Processor **(B)** Array Processor
(C) Von Neumann **(D)** All of the above

j. In Boolean expression A+BC equals

(A) $(A+B)(A+C)$ **(B)** $(A'+B)(A'+C)$
(C) $(A+B)(A'+C)$ **(D)** (A+B)C

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. What is Excitation Table. List the Excitation Tables for SR-FF, JK-FF, D-FF and T-FF. **(6)**

b. Simplify the Boolean function F together with don't care condition D in
(i) Sum of Products (ii) Product of Sums
$F(w,x,y,z)=\sum(0,1,2,3,7,8,10)$
$D(w,x,y,z)=\sum(5,6,11,15)$
(10)

Q.3 a. Design a 3×8 decoder with the help of two 2×4 decoders. **(6)**

b. Design a Binary Incrementer and Binary Decrementer.
(10)

Q.4 a. How does a basic computer handle an interrupt? Explain what happens during the interrupt with

the help of an example. Also, give the register transfer statements. **(10)**

b. Explain all the phases of instruction cycle. **(6)**

Q.5 a. Explain working of Two Pass assembler. (explain both pass1 and pass2 with flow chart). **(10)**

b. Write an assembly language program to multiply two positive numbers by a repeated addition method. For example to multiply 7 * 4 the program evaluated the product by adding 7 four times. **(6)**

Q.6 a. Differentiate between the following:

(i) Autoincrement and Autodecrement addressing mode.

(ii) Program interrupt and Subroutine call & return. **(6)**

b. What is a microinstruction? Write a microinstruction code format and explain all the fields in it. **(5)**

c. What is a microprogram? Write a microprogram for the fetch routine. **(5)**

Q.7 a. Formulate a four segment instruction pipeline for a computer. Specify the operation to be performed in each segment. **(8)**

b. Show the memory organization (1024 bytes) of a computer with four 128×8 RAM Chips and 512×8 ROM Chip. How many address lines are required to access memory. **(8)**

Q.8 a. Write a general algorithm and flow chart for addition and subtraction of two signed magnitude Numbers. **(12)**

b. Ram wants to purchase a bicycle. The bicycle must have brakes. The bicycle which has either a hand brake or foot brake. No bicycle has both type of brakes. Implement the same using basic gates. **(4)**

Q.9 Write short notes on followings

(i) Daisy chaining priority.

(ii) Direct Memory Access.

(iii) Handshaking method for data transfer.

(iv) Associative Memory. **(4*4 = 16)**