Code: C-07/T-07 **Subject: COMPUTER ARCHITECTURE**
Time: 3 Hours **Max. Marks: 100**

NOTE: There are 11 Questions in all.

- **Question 1 is compulsory and carries 16 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Answer any THREE Questions each from Part I and Part II. Each of these questions carries 14 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: (2x8)

a. Which logic is known as universal logic?

(A) PAL logic **(B)** NAND logic
(C) MUX logic **(D)** Decoder logic

b. The time for which the D-input of a D-FF must not change after the clock is applied is known as

(A) Hold time. **(B)** Set-up time.
(C) Transition time. **(D)** Delay- time.

c. How many memory chips of (128×8) are needed to provide a memory capacity of 4096×16 ?

(A) 64 **(B)** 16
(C) 32 **(D)** None of these

d. In addition of two signed numbers, represented in 2's complement form generates an overflow if

(A) $A \cdot B = 0$ **(B)** $A \oplus B = 0$
(C) $A \oplus B = 1$ **(D)** $A + B = 1$
Where A is the carry in to the sign bit position and B is the carry out of the Sign bit position.

e. Addition of $(1111)_2$ to a 4 bit binary number 'A' results:-

(A) Incrementing A **(B)** Addition of $(F)_H$
(C) No change **(D)** Decrementing A

f. In a microprocessor system, suppose, TRAP, HOLD, RESET Pin got activated at the same time, while the processor was executing some instructions, then it will first respond to

(A) TRAP **(B)** HOLD
(C) RESET **(D)** None

g. Pseudo instructions are

(A) Machine instructions. **(B)** Logical instructions.
(C) Micro instructions. **(D)** Instructions to assembler.

h. An attempt to access a location not owned by a Program is called

(A) Bus conflict. **(B)** Address fault.
(C) Page fault. **(D)** Operating system fault.

PART I

Answer any THREE Questions. Each question carries 14 marks.

Q.2 a. Design a two bit count down counter with two flip-flop and one input x. When x = 0, the state of the Flipflop does not change. When x = 1, the state sequence is 11, 10, 01, 00, 11 and repeats. **(6)**

b. Design a combinational circuit with three inputs x, y, z and three outputs A, B, C. When the binary input is 0, 1, 2 or 3, the binary output is two greater than the input. When the binary input is 4, 5, 6 and 7, the binary output is one less than the input. **(6)**

c. If $Y = \sum (m_0, m_2, m_3, m_5, m_7) + \sum d(m_6, m_9, m_{12}, m_{15})$ where 'd' stands for don't care. Express the Boolean expression in Product of Sum form and also show the K-map for that Product of Sum form. **(2)**

Q.3 a. A RAM chip 4096×8 bits has two enable lines. How many pins are needed for the integrated circuit Package? Draw a block diagram and label all input and outputs pins of the RAM. What is the main feature of random access memory? **(6)**

b. The RAM IC as described above is used in a microprocessor system, having 16 bit address line and 8-bit data line. It's enable-1 input is active when A_{15} and A_{14} bits are 0 & 1 and enable-2 input is active when A_{13}, A_{12} bits are 'X' and 'O'. What shall be the range of addresses that is being used by the RAM. **(4)**

c. Implement a full substractor logic by using 4:1 mux. **(4)**

Q.4 a. Derive the circuit for a 3 bit parity generator and 4-bit parity checker using an even parity bit. **(4)**

b. What is micro operations? Give suitable examples of some four types of micro operations. **(3)**

c. Give the hardware realization of 4-bit arithmetic circuit capable of doing addition, substraction, increment, decrement etc. Give the function table and explain its operation. **(7)**

Q.5 a. Give the comparison between & examples of hardwired control unit and microprogrammed control unit. **(4)**

b. What do you mean by Fetch cycle, instruction cycle, machine cycle, interrupt acknowledgement cycle. **(6)**

c. Explain in brief, how a digital computer system works in a interrupt driven input-output programming. **(4)**

Q.6 Design a CPU that meets the following specifications:

It can access 64 words of memory, each word being 8-bit long. The CPU does this by outputting a 6-bit address on its output pins A[5,…..0] and reading in the 8-bit value from memory on inputs D[7,…..0]. It has one 8-bit accumulator, 8-bit address register, 6-bit program counter, 2-bit instruction register, 8-bit data register.

The CPU must realise the following instruction set: **(14)**

Instruction	Instruction Code	Operation
ADD	00 AAAAAA	AC ← AC +M [AAAAAA]
AND	01 AAAAAA	AC ← AC ^M [AAAAAA]
JMP	10 AAAAAA	Go to AAAAAA
INC	11 xxxxxx	AC ← AC + 1

PART II

Answer any THREE Questions. Each question carries 14 marks.

Q.7 a. What do you mean by software & hardware interrupts? How these are used in a microprocessor system? **(5)**

b. What are the reasons of Pipe-Line conflits in a Pipe Lined processor? How are they resolved? **(5)**

c. Explain the difference between a subroutine & macro. **(4)**

Q.8 a. With neat block diagram explain the working of a microprogram sequencer for control memory. **(7)**

b. Discuss different methods used for specifying micro operations in micro operation field of micro code. State their merits and demerits. **(7)**

Q.9 a. With neat flow chart, explain the procedure for division of floating point numbers carried out in a computer. **(8)**

b. Give the flow table for register contents used in implementing booth's algorithm for the multiplier = -6 and multiplicant = +5. **(6)**

Q.10 a. What do you mean by initialisation of DMA controller? How DMA controller works? Explain with suitable block diagram. **(7)**

b. The access time of a cache memory is 120 ns and that of main memory 900 ns. It is estimated that 80% of the memory requests are for read and remaining 20% for write. The hit ratio for read access only is 0.9. A write-through procedure is used

(i) What is the average access time of the system considering only memory read cycles?

(ii) What is the hit ratio taking in to consideration the write cycles?

(iii) What is the average access time of the system for both read and write requests. **(7)**

Q.11 Write short notes on any **TWO** of the followings:-

(i) DMA data transfer.

(ii) Handshaking method of data transfer.

(iii) Isolated Vs memory mapped I/O.

(iv) RISC architecture. **(7 x 2 = 14)**