5/1/12 Code: A-20

## Diplete - ET/CS (NEW SCHEME) - Code: DE58 / DC58

10)

**Subject: LOGIC DESIGN** 

**JUNE 2009** 

Time: 3 Hours Max. Marks: 100

NOTE: There are 9 Questions in all.

- Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.
- Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

Q.1 Choose the correct or the best alternative in the following:	(2×
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- a. In a Digital Computer, binary subtraction is performed using
  - (A) 1's complement

(B) 2's complement

(C) 9's complement

- (D) 10's complement
- b. The binary equivalent of octal number 347 is
  - **(A)** 11100111

**(B)** 11011011

**(C)** 11100011

- **(D)** 11000111
- c.  $AB + \overline{AC} + BC$  is equivalent to
  - **(A)** AB+BC

**(B)** AC

(C)  $\overline{A}C + BC$ 

- **(D)**  $AB + \overline{A}C$
- d. The output of a gate is 1, if and only if odd number of inputs are at logical ones. It is true for
  - (A) OR gate

(B) NOR gate

(C) EX-OR gate

- (D) EX-NOR gate
- e. In a sequential circuit, the output at any instant depends on
  - (A) Present inputs

- **(B)** Previous outputs
- **(C)** Previous inputs and present outputs
- (D) Previous outputs and present inputs
- f. The Schmitt trigger circuit behaves as a
  - (A) Square wave generator
- **(B)** Monostable Multivibrator
- **(C)** Bistable Multivibrator
- (D) Free-running Multivibrator
- g. A mask programmed ROM is
  - (A) Programmed at the time of fabrication
  - **(B)** Programmed by the user
  - (C) Erasable and programmable

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(D) Electrically Erasa	ble.
h In a counter circuit cou	ารเร

h. In a counter circuit consisting of four JK flipflops, if all flipflops get triggered simultaneously, then it is a

- (A) Asynchronous circuit
- (B) Synchronous circuit
- (C) Combinational circuit
- (D) May be combinational or sequential circuit

i. The output Expression of Exclusive-NOR gate is

(A) 
$$A\overline{B} + \overline{A}B$$

**(B)** 
$$AB + \overline{A} \overline{B}$$

(C) 
$$\overline{AB} + \overline{A} \overline{B}$$

- **(D)** None of the above
- j. The minimum number of flipflops required for a synchronous decade counter is
  - **(A)** 10

**(B)** 2

**(C)** 4

**(D)** 3

## Answer any FIVE Questions out of EIGHT Questions. Each question carries 16 marks.

Q.2 a. Explain the operation of digital computer with block diagram

**(7)** 

- b. Perform the following conversions:
  - (i)  $(237)_{16}$  to Octal (ii)  $(375)_{10}$  to Hexa decimal (iii)  $(11110000110)_2$  to Decimal
- (9)

Q.3 a. State and prove the Demorgan's Theorems

**(8)** 

- b. Simplify the expressions and realise using basic gates
  - (i)  $XY + XYZ + XY\overline{Z} + \overline{X}YZ$
  - (ii) Use K-map to simplify,  $Y = \overline{C}(\overline{A} \overline{B} \overline{D} + D) + \overline{A} \overline{B} C + \overline{D}$
- **(8)**
- **Q.4** a. Explain the operation of internal circuit of edge triggered JK flipflop with truth table.
- (8)

- b. With waveforms explain Serial data transfer of 4-bit Shift Register.
- (8)

Q.5 a. Design one bit full adder circuit

(8)

b. Perform the following:

(8)

- (i) 2's complement subtraction: 120-55
  - (ii) BCD addition: 275+641
- **Q.6** a. With truth table and block diagram. Explain synchronous Mod-16 counter.
- **(8)**
- b. Design Mod-12 asynchronous counter that counts binary sequence 0000 through 1011. Also draw the waveforms.
  - (3
- Q.7 a. What is multiplexer? Explain any two applications of multiplexers.
- **(8)**
- b. Define Magnitude comparator? Show how 74HC85 four bit Magnitude Comparator can be used to perform 8-bit comparison. (8)

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<b>Q.8</b>	a.	Explain Mod-6 Johnson counter with block diagram and waveforms.	(8	3)
V.0	u.	Explain frod 0 Johnson Council with block diagram and wavelones.	,,,	,

b. Show how to connect 74ALS174 as a Serial Shift register with data shifting on each PGT of clock pulse as follows:  $D_5 \rightarrow D_4 \rightarrow D_3 \rightarrow D_2 \rightarrow D_1 \rightarrow D_0$ . Name any four applications of shift registers. (8)

## **Q.9** a. Define the following:

- (i) Memory cell (ii) Byte (iii) Access time (iv) Address (8)
- b. With the help of NMOS cell, explain the operation of static RAM. Draw timing diagram for static RAM Read cycle. (8)