DiplETE – ET/CS (NEW SCHEME) – Code: DE58 / DC58

Subject: LOGIC DESIGN

Time: 3 Hours **Max. Marks: 100**

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions, answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2 10)

a. The term bit means

(A) a small amount of data **(B)** a 1 or a 0
(C) binary digit **(D)** both answers (B) or (C)

b. The BCD number for decimal 473 is

(A) 111 0 11010 **(B)** 11000 1110011
(C) 01000111 00 11 **(D)** 01001111 0011

c. The out put of a gate is low when at least one of its input is low. It is true for

(A) AND **(B)** OR
(C) NAND **(D)** NOR

d. Which one of the following is not a valid rule of Boolean algebra?

(A) A+1 = A **(B)** A+0 =
(C) A = 0 **(D)** AA = A

e. The AND operation can be produced with

(A) two NAND gates **(B)** three NAND gates
(C) one Nor gate **(D)** two Nor gates

f. A 4- bit parallel adder can add

(A) two 4 – bit binary numbers. **(B)** two-2-bit binary numbers
(C)four bit at a time **(D)** four bite in sequence

g. A modules -10 Johnson counter requires

(A) ten flip flops **(B)** four flip- flops
(C) five flip flops **(D)** eight-flip-flops

h. The purpose of the clock input- to a flip flop is to

(A) Clear the device
(B) sell-the device
(C) always cause the out put to change states
(D) cause the out to change the states only after both the input change.

i. An asynchronous counter differs from a synchronous counter in
(A) the number of states in its sequence
(B) the method of clocking
(C) the type of flip-flop used
(D) the value of the modulus.

j. A memory with 256 addresses has
(A) 256 address lines **(B)** 6 address lines
(C) 4 address lines **(D)** 8 address lines

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Perform the following
(i) $(18.665)_{10} = (?)_{8}$ (ii) $(101011.011)_2 = (?)_{16}$
(iii) $(ABC.DE)_{16} = (?)_{10}$ (iv) $(763)_8 = (?)_{16}$ **(8)**

b. Explain parity method for error detection **(8)**

Q.3 a. State and prove the De-Morgan's Theorems **(8)**

b. use a Karnaugh map to reduce the following expressions and realize the functions using minimum number of NAND gates.
(i) + D + ABCD + ABC
(ii) AB + A C +ABC **(8)**

Q.4 a. Explain the following:
(i) D flip flop (ii) SR flip flop **(8)**

b. Explain how flip flops can be used to store parallel data. Explain the set-up and hold-up time in a flip flop. **(8)**

Q.5 a. Perform the following subtraction by 2's complement system **(6)**
(i) 15 – 23 (ii) 32 – 18

b. Represent $(59)_{10}$ and $(38)_{10}$ in BCD and perform BCD addition. Verify the result by converting back to decimal. **(6)**

c. Show how 2's complement method of subtraction can be performed by using IC 7483 (parallel adder) and explain the same. **(4)**

Q.6 a. Draw the logic diagram of IC 74293 and show that how this counter can be used as modulus -12 counter. **(8)**

b. Design a 4-bit binary counter. **(8)**

Q.7 a. Design a full adder by using 4: 1 multiplexer. **(8)**

b. Explain how a de multiplexer is converted into decoder. **(4)**

c. Design a 1 – bit comparator. **(4)**

Q.8 a. Draw the circuit diagram of a 4- bit Johnson counter and explain the operation with neat waveform. Also mention its merits and demerits. **(8)**

b. Explain IC 74165, parallel in/ serial out shift register with its logic diagram. **(8)**

Q.9 a. Define these terms
(i) Access time.
(ii) Read only Memory.
(iii) Elastic memory devices.
(iv) SRAM and DRAM. **(8)**

b. With neat diagram explain Intel 2864 EEPROM. **(8)**