Total No. of Questions—**12**] [Total No. of Printed Pages—**4**

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S.E. (Electrical) (First Sem.) EXAMINATION, 2010

ANALOG AND DIGITAL ELECTRONICS

(2008 COURSE)

Time : Three Hours **Maximum Marks : 100**

N.B. **:—** (*i*) Answer any *three* questions from each Section.

(*ii*) Answers to the two Sections should be written in separate answer-books.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Use of logarithmic tables, slide rule, Mollier charts, electronic pocket calculator and steam tables is allowed.

(*vi*) Assume suitable data, if necessary.

SECTION I

1. (*a*) Explain input-output characteristics of CE configuration with neat connection diagram and characteristic curve. [10]

(*b*) Explain AC-DC load line analysis using common emitter configuration. [8]

Or

2. (*a*) Draw and explain multistage amplifier. Also state advantages and applications. [6]

P.T.O.

(*b*) Define the following terms associated with FET :

(*i*) Transconduction

(*ii*) Amplification factor. [4]

(*c*) What is significance of transfer and drain characteristics of FET ? Draw and explain. [8]

3. (*a*) Explain with neat diagram Schmitt trigger as an application of op-amp. [8]

(*b*) Explain grounded type load voltage to current converter. [8]

Or

4. (*a*) What is the role of op-amp as an instrumentation amplifier ? Explain 3-op-amp instrumentation amplifier. [8]

(*b*) Explain open loop and close loop configuration of op-amp. [8]

5. (*a*) Draw and explain monostable multivibrator. Also state applications. [8]

(*b*) Using LM317 explain variable voltage regulator with neat diagram. [8]

Or

6. (*a*) Explain sine wave generator using op-amp. Draw output w/fs. [8]

(*b*) Explain with neat connection diagram low pass filter. [8]

SECTION II

7. (*a*) Convert the following numbers into equivalent BCD : [6]

(*i*) $(11011011)_2$

(*ii*) $(333)_8$

(*iii*) $(DB)_{16}$

(*b*) State De Morgan's theorem and using Boolean algebra prove the following : [6]

$$(\overline{A} + B)\,(A + B + D)\,\overline{D} = B\overline{D}\,.$$

(*c*) Explain Excess-3 code in detail. [6]

Or

8. (*a*) If

$$f = \sum m(4,5,6,7,8,12) + d(1,2,3,9,13,14)$$

using K-map reduce expression and realise using logic gates. [6]

(*b*) Explain binary number system in detail. Also give the difference between binary number system and BCD. [6]

(*c*) Design 1-bit comparator using K-map and realise it using logic gates. [6]

9. (*a*) Explain J-K flip-flop in detail with input and output wave-forms. Also give the functions of preset and clear pin. [8]

(*b*) Design and explain MOD 5 asynchronous counter with related timing diagram. [8]

Or

10. (*a*) Design 3-bit synchronous up counter using J-K flip-flops and K-map. [8]

(*b*) Explain edge triggered and level triggered flip-flops. Also explain D-flip-flop in detail. [8]

11. (*a*) Explain 1 : 4 demultiplexer along with logic diagram and truth table. [8]

(*b*) Explain dual slope ADC in detail. [8]

Or

12. Write short notes on : [16]

(*i*) Static RAM

(*ii*) Dynamic RAM

(*iii*) EPROM

(*iv*) EEPROM.