Code No: R5310201 **R5**

III B.Tech I Semester(R05) Supplementary Examinations, November 2010
COMPUTER ORGANIZATION
(Common to Electrical & Electronics Engineering, Electronics & Communications Engineering, Electronics & Instrumentation Engineering and Electronics & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Find the actual number from its IEEE 754 representation.
Sign = 0
Exponent = 1000 0000
Mantissa = 1100 0000 0000 0000 0000 000 [6]
(b) What is meant by normalization in floating point representation? Why do we need it? What is bias? What normalization is used in IEEE 754 standard? [10]

2. Design register selection circuit to select one of the four 4-bit registers content on to bus. Give fuller explanation. [16]

3. (a) What are the design goals for a designer while deciding a hardwired or microprogrammed CU for a CPU. [8]
(b) Explain nanoinstructions and nanometry. Why do we need them. [8]

4. (a) How many bits are needed to store the result addition, subtraction, multiplication and division of two n-bit unsigned numbers. Prove. [8]
(b) What is overflow and underflow. What is the reason?. If the computer is considered as infinite system do we still have these problems?. [8]

5. (a) What is the functioning of a Flash Memory? Explain. [8]
(b) Give the detailed picture of Memory Hierarchy. [8]

6. (a) What are the different types of I/O communication techniques? Give brief notes.
(b) In the above techniques, which is the most efficient? Justify your answer. [8+8]

7. Explain the following with related to the Instruction Pipeline
(a) Pipeline conflicts
(b) Data dependency
(c) Hardware interlocks
(d) Operand forwarding
(e) Delayed load
(f) Pre-fetch target instruction
(g) Branch target buffer
(h) Delayed branch [8×2=16]

8. (a) What is the functioning of cross bar switch network? Explain. With a neat sketch [12]
(b) How many switch points are there in a cross bar switch network that connect 'p' Processors to 'm' Memory modules. [4]

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