Name : .....

Roll No. : .....

Invigilator's Signature : .....

2010

ADVANCED COMPUTER ARCHITECTURE

Time Allotted : 3 Hours Full Marks : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : 10 × 1 = 10

i) A computer with cache access time of 100 ns and hit ratio of 0·9 produces an average access time of

a) 250 ns b) 200 ns

c) 190 ns d) none of these.

ii) Which of the following is example of 2-dimensional topologies in static network ?

a) Mesh b) $3C^3$/ Network

c) Linear Array d) None of these.

iii) Advantage of MMX technology lies in

a) Multimedia application

b) VGA

c) CGA

d) none of these.

iv) Array Processor is present in

a) SIMD b) MISD

c) MIMD d) none of these.

v) Basic difference between Vector and Array processors is

a) pipelining

b) interconnection network

c) register

d) none of these.

vi) Stride in Vector processor is used to

a) differentiate different data types

b) registers

c) differentiate different data

d) none of these.

vii) Which one of the following has no practical usage ?

a) SISD b) SIMD

c) MISD d) MIMD.

viii) Difference between RISC and CISC is

a) RISC is more complex

b) CISC is more effective

c) RISC is better optimizable

d) none of these.

ix) For 2 instructions I and J, WAR hazard occurs if

a) $R(I) \cap D(J) \neq \phi$ b) $R(I) \cap R(J) \neq \phi$

c) $D(I) \cap R(J) \neq \phi$ d) none of these.

x) The seek time of a disk is 50 ms. It rotates at the rate of 30 rotations/second. The capacity of each track is 300 words. The access time is approximately

a) 62 ns b) 60 ns

c) 47 ns d) none of these.

GROUP – B
(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Describe Flynn's classification of parallel computers.

3. Differentiate between C-access and S-access memory organizations.

4. What are the different factors that can affect the performance of a pipelined system ? Differentiate between WAR and RAW hazards. $2 + 3$

5. Assume that main memory size is of 32 kB × 12. Cache memory size is of 512 × 12 and block size is of 1 word. Describe the following :

   a) Direct mapping technique

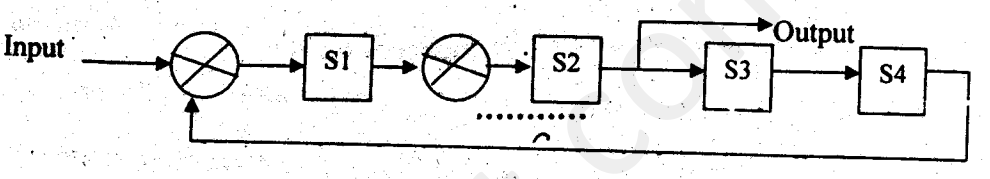
   b) Associative mapping technique. $2\frac{1}{2} + 2\frac{1}{2}$

6. Compare between RISC and CISC.

GROUP – C
(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) Consider the four stage pipelined processor specified by the following diagram :



This pipeline has a total evaluation time of six clock cycles. All successor stages must be used after each clock cycle.

i) Specify the reservation table for above pipelined processor with six columns and four rows.

ii) What are the forbidden latencies and the initial collision vector ? Draw the state transition diagram.

iii) Determine all simple cycles, greedy cycle and MAL.

iv) Determine the throughput of this pipelined processor. Given clock period as 20 ns.

b) What do you mean by pipelined chaining ? Define the various types of vector instructions. (2 + 4 + 3 + 2) + 4

8. a) What is cache memory ? Define global miss & local miss with a suitable example.

   b) Describe different techniques to reduce Miss Penalty.

   c) Describe different techniques to reduce Miss Rate.

(2 + 5) + 4 + 4

9. a) What do you mean by multiprocessor system ? What are the similarities and dissimilarities between the multiprocessor system and multiple computer system ?

   b) What are the different architectural models for multiprocessors ? Explain each of them with example.

   c) Distinguish between loosely coupled and tightly coupled multiprocessor architectures. Which architecture is better and why ? 5 + 5 + 5

10. a) Write a short note on vectorizing compliers.

    b) What are strip mining and vector stride, in respect of vector processors ?

    c) Both vector processors and array processors are specialized to operate on vectors. What are the main differences between them ? 5 + 5 + 5

11. Write short notes on any *three* of the following : 3 × 5

a) Power PC

b) Memory to memory vector architecture

c) Array processor

d) Memory inclusion

e) Memory interleaving.