

A4-R3: COMPUTER ORGANIZATION

NOTE:

1. There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions.
2. **PART ONE** is to be answered in the **TEAR-OFF ANSWER SHEET** only, attached to the question paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book.
3. Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates, who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE**.

TOTAL TIME: 3 HOURS

TOTAL MARKS: 100
(PART ONE – 40; PART TWO – 60)

PART ONE

(Answer all the questions)

1. **Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the “tear-off” answer sheet attached to the question paper, following instructions therein.** (1 x 10)
 - 1.1 Octal equivalent of hexadecimal code F3A1 is
 - A) 173101
 - B) 176541
 - C) 171641
 - D) 158661
 - 1.2 The O/P states of three-state bus buffer are
 - A) 1, 2, 3
 - B) 0, 1, 2
 - C) 0, 1, High Impedance
 - D) None of the above
 - 1.3 Which of the following shift operations multiply a signed binary number by 2?
 - A) Logical shift left
 - B) Logical shift right
 - C) Arithmetic shift left
 - D) Arithmetic shift right
 - 1.4 In Computation type instructions the address of the operand and in branch-type instructions the target address is known as:
 - A) Effective Address
 - B) Indirect Address
 - C) Direct Address
 - D) Associative Address
 - 1.5 The half adder performs
 - A) Decimal addition operation for 2 decimal inputs
 - B) Binary addition operation for 2 binary inputs
 - C) Decimal addition operation for 2 binary inputs
 - D) Binary addition operation for 2 decimal inputs

- 1.6 A Decoder is a combinational circuit that converts binary information from the N coded inputs to a maximum of
- A) 2^{N-1} unique outputs
 - B) 2^{2N} unique outputs
 - C) 2^{N+1} unique outputs
 - D) None of the above
- 1.7 Shift instructions are
- A) Data manipulation instructions
 - B) Data transfer instructions
 - C) Program control instructions
 - D) All of the above
- 1.8 The smallest number which can be represented as signed number (using 2's complement) in 1 byte is
- A) $-2^8 - 1$
 - B) 0
 - C) $-2^8 + 1$
 - D) -2^8
- 1.9 An assembler is a program, which generates
- A) An executable program from object programs
 - B) An executable program from assembly language programs
 - C) An assembly language program from a high level language programs
 - D) An executable program from a high level language programs
- 1.10 Cycle stealing refers to
- A) Reduction in the number of clock cycles for memory access in a cache memory
 - B) Overlapping of the memory refresh operation and memory read operation in dynamic memory
 - C) Reduction in instruction cycle time through instruction pipelining
 - D) None of the above

2. Each statement below is either TRUE or FALSE. Choose the most appropriate one and ENTER in the “tear-off” sheet attached to the question paper, following instructions therein. (1 x 10)

- 2.1 The following operation is known as memory read operation:

$$DR \leftarrow M[AR]$$
- 2.2 The idea of virtual memory is based on principal of locality of reference.
- 2.3 DMA is used to transfer data from main memory to cache memory.
- 2.4 A flip-flop is binary cell capable of storing of eight bits of information.
- 2.5 Memory stack can be implemented in a Random Access Memory attached at CPU.
- 2.6 Use of PC register in a basic computer organization is to store instruction.
- 2.7 In arithmetic addition, overflow condition can be detected by observing the carry out of the sign bit position only.
- 2.8 Virtual memory can be larger than physical memory.
- 2.9 A multiplexer is a combinational circuit that receives binary information from one of 2^N input data and directs it to N output line.
- 2.10 In microprogrammed control, the control logic is implemented with gates, flip-flops, decoders and other combinational circuit.

3. Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the “tear-off” answer sheet attached to the question paper, following instructions therein. (1 x 10)

X		Y	
3.1	Execution of instructions divided into phases	A.	Analog Circuit
3.2	ROM	B.	Output Device
3.3	AC	C.	Immediate addressing mode
3.4	Keyboard	D.	Arithmetic Pipelining
3.5	Operands are data instead of Address in	E.	Volatile Memory
3.6	DMA	F.	Direct Addressing Mode
3.7	Register Transfer Language	G.	Instruction pipelining
3.8	Monitor	H.	It uses cycle stealing to transfer data
3.9	It stores address of next instruction	I.	Accumulator
3.10	RAM	J.	System Level Language
		K.	Input Device
		L.	Symbolic Notation
		M.	Non-Volatile Memory
		N.	Program Counter

4. Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Enter your choice in the “tear-off” answer sheet attached to the question paper, following instructions therein. (1 x 10)

A.	Full	B.	Multiply	C.	First
D.	RAM	E.	N	F.	Same
G.	Divide	H.	Microprogrammed control	I.	N-1
J.	Stack	K.	Instruction Code	L.	Half
M.	Hard-wired	N.	HDD	O.	Write through
P.	Different	Q.	Operation Code	R.	Write back

- 4.1 Operation code must consist of at least _____ bits for 2^N (or less) distinct operations.
- 4.2 In _____, the control information is stored in control memory rather than implemented in combinational circuit.
- 4.3 The procedure to update main memory along with cache memory at every write operation is called _____.
- 4.4 In _____ the process of locating a word in a memory is the same and requires equal amount of time no matter where the cells are located in physical memory.
- 4.5 A combinational circuit that performs the arithmetic addition of three bits is called _____ adder.
- 4.6 A(n) _____ is a group of bits that instruct the computer to perform a specific operation.
- 4.7 Asynchronous I/O transfer schemes operate from _____ clock.
- 4.8 In two pass assembler, the address symbol table is generated in _____ pass.
- 4.9 In zero address instructions, operands come from _____.
- 4.10 Booth algorithm is used to _____ two signed magnitude data.

PART TWO
(Answer any **FOUR** questions)

- 5.**
- a) Control Unit in processor generates time and control signals to control other devices in computer. How does control unit of CPU generate time and control signal based on the instructions? Explain it with necessary diagram.
 - b) What is meant by Digital Logic Gates? Give the name, Graphical symbol, algebraic function and truth table of basic logic gates.
 - c) Using two complements method, perform subtraction of the following unsigned binary numbers: 1010100 - 1010100
- (7+5+3)**
- 6.**
- a) What are the memory reference instructions? Explain any three memory reference instructions.
 - b) Using two address instructions, write a program in symbolic notation to evaluate the following arithmetic statement:
$$X = A - B + C * (D * E - F) / G + H - K$$
 - c) A typical digital computer has many registers and paths must be provided to transfer information from one register to another register using a common bus. Using multiplexers, design combinational circuit which puts 4-bits of data from any one of four registers of digital computer on common bus.
- (5+4+6)**
- 7.**
- a) Draw and explain hardware algorithm to perform the addition and subtraction of two numbers in signed magnitude form.
 - b) Draw and explain circuit of a bidirectional shift register with parallel load with the help of D flip-flops and 4 x 1 multiplexer.
- (10+5)**
- 8.**
- a) Explain the functioning of magnetic disk storage device.
 - b) Give the difference between macro and subroutine.
 - c) How, DMA is connected to RAM, CPU and I/O peripherals? Draw a diagram of DMA transfer and explain its working.
- (4+4+7)**
- 9.**
- a) Explain the working of a Dot Matrix printer.
 - b) The transformation of data from main memory to cache is referred as mapping process. Taking a suitable example, explain direct mapping from main memory to cache.
- (5+10)**