B.Tech Degree III SemesterExamination & November 2002

IT 304 ELECTRONIC CIRCUITS AND LOGIC DESIGN

(1999 Admissions onwards)

| Time: 3 Hours | | Max. Marks: | ks: 100 | |
|---------------|------------|--|------------|--|
| I. | (a) | Draw a typical circuit of R.C. Coupled Amplifier with negative feed back. | (4) | |
| | (b) | Design the circuit for voltage gain of 5. | (8) | |
| | (c) | Explain the conditions for sustained oscillations. How is it achieved in R.C. phase | | |
| | | shift oscillators? | (5) | |
| | (d) | Define Class A, Class B and Class C operations. | (3) | |
| | | OR | | |
| II. | (a) | Draw a typical R.C. coupled amplifier and obtain expression for current gain at low, | žO. | |
| | 4. | and medium frequencies. | (8) | |
| | (b) | Explain with necessary diagram a pushpull amplifier. | (6) | |
| | (c) | Compare with necessary circuit diagrams the working of R.C. phase shift and Wein | (6) | |
| | | bridge oscillators. | (6) | |
| Ш, | (a) | Explain with necessary diagrams and expressions working of SCR. | (8) | |
| | (b) | Give its applications. | (2) | |
| | (c) | Define CMRR. Draw the block schematic of an operational amplifier and explain. | (6) | |
| | (d) | Draw a circuit to obtain sharp pulses from the given sinusoidal signal at 100 Hz. | (4) | |
| | • • | OR | | |
| IV. | (a) | Explain what is meant by "drift" and "offset" in connection with operational amplifiers. | (4) | |
| | (b) | Explain the working of UJT. How it can be used in oscillators. | (8) | |
| | (c) | Derive expressions for good differentiation and integration using R and C. | | |
| | | | (8) | |
| V. | (a) | Realise using NAND gates | | |
| | | $f(ABCD) = \sum_{i=1}^{n} [0,1,2,4,8,10,11]$ | | |
| | | don't cares = [3,6,13] | (8) | |
| | (b) | Realise in POS form | | |
| | (0) | $f(ARCD) = \Pi[1 \ A \ 5 \ 7 \ 12 \ 14 \ 15]$ | | |
| | | $f(ABCD) = \prod_{M} [1, 4, 5, 7, 12, 14, 15]$ | | |
| | | don't cares = [3,6] | (8) | |
| | (c) | What is meant by Max terms? Give examples. | (4) | |
| VI. | (m) | OR | | |
| V1. | (a) | Simplify using K-map and realise using minimum number of NAND gates. | | |
| | | f(ABCD) = ABCD + BCD + AB + AB + AC | (8) | |
| | (b) | Explain with examples binary division process. | (8) | |
| | (c) | What is parity checking? | (4) | |
| | | | | |
| VII. | (a) | Draw a typical TTL circuit and explain its working. | (9) | |
| | (b) | What are the problems faced in interfacing TTL to CMOS? | (9) | |
| | (c) | Define noise margin in TTL. | (2) | |
| 3.7777 | | OR | | |
| VIII. | (a) | Draw the circuit of a typical up/down synchronous counter and give its truth table | (10) | |
| | (L) | and waveforms with explanations. | (10) | |
| | (b) (c) | Differentiate between combinational and sequential circuits. Draw a typical D Flip flop and explain its salient features. | (6) (4) | |
| | (0) | Draw a typical D Filp flop and explain its salient leadines. | (+) | |
| IX. | (a) | Differentiate between PLA and PAL | (12) | |
| | (b) | Draw a typical BJTRAM cell and explain. | (8) | |
| | (-) | OR | \-/ | |
| Х. | (a) | Explain with examples typical Decoder, Demultiplexer and Multiplexer. | (14) | |
| | (b) | Draw a typical EPROM cell and explain its working. | (6) | |