Code No: R05210504 **Set No. 2**

II B.Tech I Semester Regular Examinations, November 2008
DIGITAL LOGIC DESIGN
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Perform the following using BCD arithmetic. [4+4]
   i. $1263_{10} + 9687_{10}$
   ii. $7672_{10} + 3378_{10}$

   (b) Convert the following:
   i. $997_{10} = (\quad)_{16}$
   ii. $257_{10} = (\quad)_{8}$
   iii. $654_{10} = (\quad)_{2}$
   iv. $101_{16} = (\quad)_{10}$ [2+2+2+2]

2. (a) Express the following functions in sum of minterms and product of maxterms.
   i. (xy + z) (y + xz)
   ii. B'D + A'D + BD.

   (b) Obtain the complement of the following Boolean expressions. [8+8]
   i. AB'C + AB'D + A'B'
   ii. A'B'C + ABC' + A'B'C'D
   iii. ABCD + ABC'D? + A'B'CD
   iv. AB + ABC'.

3. (a) If
   $F_1(A, B, C) = A \oplus B \oplus C$
   $F_2(A, B, C) = A \Theta C \Theta B$
   Show that $= F_1 = F_2$

   (b) Show that $A \oplus B \oplus AB = A + B$

   (c) Obtain minimal SOP expression for the complement of the given expression: $F(A, B, C) = \prod (1, 2, 5, 7)$ And draw the circuit using NOR - gates. [4+4+8]

4. (a) A multiple output combinational logic circuit is defined by the following functions. Draw the schematic circuits for F_1 and F_2.
   $F_1(A, B, C, D) = \overline{\overline{A} \bullet \overline{\overline{A}D}} \bullet \left(\overline{A} + BC\right)$
   $F_2(A, B, C, D) = \overline{\overline{A}D} \bullet \left(\overline{A} + BC\right)$
   Using K-Maps simplify F_1 and F_2 and draw the reduced diagram circuit.

(b) Design a full - subtractor circuit with three inputs x,y,z and outputs D, B. The circuit subtracts X - Y - Z where Z is the input borrow, B is the output borrow and D is the difference draw the circuit using NAND gates. [8+8]

5. (a) Define the following terms related to filp-flops.
   i. set-up time
   ii. hold time
   iii. propagation delay
   iv. preset and
   v. clear.

   (b) Distinguish between combinational logic and sequential logic. [10+6]

6. (a) Design a 4-bit ring counter using T- flip flops and draw the circuit diagram and timing diagrams.

   (b) Draw the block diagram and explain the operation of serial transfer between two shift registers and draw its timing diagram. [8+8]

7. (a) Explain the block diagram of a memory unit. Explain the read and write operation a RAM can perform.

   (b) i. How many 32K * 8 RAM chips are needed to provide a memory capacity of 256K bytes.
   ii. How many lines of the address must be used to access 256K bytes? How many of these lines are connected to the address inputs of all chips?
   iii. How many lines must be decoded for the chip select inputs? Specify the size of the decoder. [8+8]

8. Reduce the number of states in the state table listed below. Use an implication table. [16]

Present state	Next state		Output	
	x=0	x=1	x=0	x=1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	0	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

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