Code No: R05210504 **Set No. 3**

II B.Tech I Semester Regular Examinations, November 2008
DIGITAL LOGIC DESIGN
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain different methods used to represent negative numbers in binary system. [6]
   (b) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend. [5×2]
      i. 11010 - 10110
      ii. 11011 - 1001
      iii. 100 - 110100
      iv. 1010101 - 1010101
      v. 11 - 1101.

2. (a) Convert the following expressions in to sum of products and product of sums.
      i. (AB + C) (B + C'D)
      ii. x' + x(x + y')(y + z').
   (b) Obtain the Dual of the following Boolean expressions. [8+8]
      i. (AB' + AC')(BC + BC')(ABC)
      ii. AB'C + A'BC + ABC
      iii. (ABC)'(A + B + C)'
      iv. A + B'C (A + B + C').

3. (a) Construct K-map for the following expression and obtain minimal SOP expression. Implement the function with 2-level NAND -NAND form.
   $f(A,B,C,D) = (A+C+D)\left(A+B+\overline{D}\right)\left(A+B+\overline{C}\right)\left(\overline{A}+B+\overline{D}\right)\left(\overline{A}+B+\overline{D}\right)$
   (b) Implement the following Boolean function F using the two - level form: [8+8]
      i. NAND-AND
      ii. AND-NOR $F(A,B,C,D) = \Sigma 0,1,2,3,4,8,9,12$

4. (a) Implement 64 × 1 multiplexer with four 16 × 1 and one 4 ×1 multiplexer. (Use only block diagram).
   (b) A combinational logic circuit is defined by the following Boolean functions.
   $F_1 = \overline{ABC} + AC$
   $F_2 = A\overline{BC} + \overline{A}B$
   $F_3 = A\overline{B}C + AB$
   Design the circuit with a decoder and external gates. [8+8]

5. A sequential circuit with 3 D-flip-flops A, B and C has only one input 'X' and one output 'X' with following relationship
   $D_A = B \oplus C \oplus X, \quad D_B = A, \quad D_C = B$

   (a) Draw the logic diagram of the circuit.

   (b) Obtain logic diagram, state table and state diagram. [16]

6. Draw the sequential circuit for serial adder using shift registers, full adder and D-FF. Explain its operation with state equations and state table . [16]

7. Derive the PLA programming table and the PLA structure for the combinational circuit that squares a 3- bit number. Minimize the number of product terms. [16]

8. (a) What do you mean by hazard? Classify and explain.

   (b) Draw the logic diagram of the product of sums expression:
   Y= (x_1 + x_2') (x_2 + x_3). Show that there is a 0-hazard when x_1 and x_3 are equal to 0 and x_2 goes from 0 to 1. Find a way to remove the hazard by adding one or more OR gate. [8+8]

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