Code No: R05210504 **Set No. 1**

II B.Tech I Semester Regular Examinations, November 2008
DIGITAL LOGIC DESIGN
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks
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1. Convert the following to Decimal and then to Hexadecimal.
   (a) 1234_8
   (b) 1267_8
   (c) 11001111_2
   (d) 11011101_2
   (e) 786_{10}
   (f) 555_{10} [3+3+3+3+2+2]

2. (a) Find the complement of the following and show that F.F' = 0 and F + F' = 1.
      i. F = xy' + x'y
      ii. F = (x + y' + z)(x' + z')(x + y).
   (b) Obtain the Dual of the following Boolean expressions. [8+8]
      i. B'C'D + (B + C + D)' + B'C'D'E
      ii. AB + (AC)' + (AB + C)
      iii. A'B'C' + A'BC' + AB'C' + ABC'
      iv. AB + (AC)' + AB'C.

3. (a) Construct K-map for the following expression and obtain minimal SOP expression. Implement the function with 2-level NAND -NAND form.
   $f(A,B,C,D) = (A + C + D)\left(A + B + \overline{D}\right)\left(A + B + \overline{C}\right)\left(\overline{A} + B + \overline{D}\right)\left(\overline{A} + B + \overline{D}\right)$
   (b) Implement the following Boolean function F using the two - level form: [8+8]
      i. NAND-AND
      ii. AND-NOR $F(A,B,C,D) = \Sigma 0, 1, 2, 3, 4, 8, 9, 12$

4. (a) Implement 64 × 1 multiplexer with four 16 × 1 and one 4 ×1 multiplexer. (Use only block diagram).
   (b) A combinational logic circuit is defined by the following Boolean functions.
   $F_1 = \overline{ABC} + AC$
   $F_2 = A\overline{BC} + \overline{A}B$
   $F_3 = A\overline{B}C + AB$
   Design the circuit with a decoder and external gates. [8+8]

5. A sequential circuit with 3 D-flip-flops A, B and C has only one input 'X' and one output 'X' with following relationship
   $D_A = B \oplus C \oplus X, \quad D_B = A, \quad D_C = B$

   (a) Draw the logic diagram of the circuit.

   (b) Obtain logic diagram, state table and state diagram. [16]

6. (a) Draw and explain 4-bit universal shift register.

   (b) Explain different types of shift registers. [8+8]

7. (a) Draw and explain the block diagram of PAL.

   (b) Implement the following Boolean functions using PAL.
   w(A,B,C,D) = Σ m (0,2,6,7,8,9,12,13)
   x (A,B,C,D) = Σ m (0,2,6,7,8,9,12,13,14)
   y (A,B,C,D) = Σ m (2,3,8,9,10,12,13)
   z (A,B,C,D) = Σ m (1,3,4,6,9,12,14). [6+10]

8. (a) Describe the operation of the SR Latch using NAND gate with the help of truth table, transition table and the circuit.

   (b) Explain the operation and use of De bounce circuit. [8+8]

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