Seat No.:	Enrollment No.
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GUJARAT TECHNOLOGICAL UNIVERSITY

B.E. Sem-III Regular / Remedial Examination December 2010

Subject code: 130704

Date:	18	Subject Name: Computer Organization and Architecture Time: 10.30 am - 01.00 pm Total Marks: 70	
 Instructions: Attempt all questions. Make suitable assumptions wherever necessary. Figures to the right indicate full marks. 			
Q.1 Q.2	(a) (b) (a)	Discuss the phases of Instruction Cycle with flowchart.	07 07 07
	(b)	Derive the control gate structure associated with the Address Register (AR) in the basic computer. OR	07
	(b)	Explain the following instructions: SPA, SNA, SZA, SZE.	07
Q.3	(a) (b)	Explain the basic working principle of the Control Unit of basic computer using diagram.	07 07
Q.3	(a) (b)		07 07
Q.4	(a) (b)	Explain the working of Second Pass Assembler with its flowchart. Write the program to multiply two positive numbers. by a repeated addition method. For ex., to multiply 5 x 4, the program evaluates the product by adding 5 four times, or 5+5+5+5. OR	07 07
Q.4	(a)		07
	(b)		07
Q.5	(a) (b)	Explain the Booth Multiplication Algorithm in detail. Explain the Instruction Pipelining with example. OR	07 07
Q.5	(a) (b)	Explain the procedure for addition and subtraction with signed-magnitude data with the help of flowchart. Draw the diagram of Micro programmed sequencer for a control memory and explain it.	07 07
