CE1-R3: ADVANCED COMPUTER ARCHITECTURE

NOTE:

1. **Answer question 1 and any FOUR questions from 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) What is meant by throughput rate? Calculate the throughput rate for a program with clock frequency 25 MHz, CPI value is 5 and construction count 100.

b) Consider the following code written for a sequential execution on a uniprocessor system:

```
L1:   DO 10 I = 1, N
L2:   A(I) = B(I) + C(I)
L3:   10 CONTINUE
L4:   SUM = 0
L5:   DO 20 I = 1, N
L6:   SUM = SUM + A(I)
L7:   20 CONTINUE
```

Write a parallel code of this program for a multiprocessor system.

c) Explain the cluster model of memory organization, with the help of a suitable diagram.

d) DMA access is given higher priority than CPU access to memory, why?

e) What is the average time to read or write a 512-byte sector for a typical disk? The specified average seek time is 9 ms, the transfer rate is 4 MB/Sec, it rotates at 7200 rpm, and the controller overhead is 1 ms. Assume the disk is idle so that there is no queuing delay.

f) Explain, briefly how RISC architecture attempts to reduce execution time.

g) How pipelining concept is implemented in superscalar processors?

(7x4)

2.

a) A computer system has a 128 byte cache. It uses a four way set associative mapping with 8 bytes in each block. The physical address size is 32 bits and smallest addressable unit is 1 byte. Draw a diagram showing the organization of the cache indicating how physical addresses are related to cache address.

b) Differentiate between asynchronous and synchronous pipeline model?

c) Vectorizing compilers generally detect loops that can be executed on a pipelined vector computer. Are the vectorization algorithms used by vectorizing compilers suitable for MIMD machine parallelization? Justify your answer.

(6+6+6)

3.

a) Explain the concept of daisy chain bus arbitration with the help of a diagram. Also make corresponding timing diagram.

b) Consider a three stage pipeline having following reservation table: -

	1	2	3	4	5	6	7	8	→ Time
S_1	X					X		X	
S_2		X		X					
S_3			X		X		X		

Find the state transition diagram corresponding to this reservation table.

c) Define the pipeline performance/cost ratio. For what purpose it is used?

(6+6+6)

4.

a) What are message passing systems? Explain the format of message, packet and fit in the context of message passing system.

b) What is meant by wormhole routing? Where is it used?

c) What are "hot spots" in context of interconnection networks? How do they affect the designing of interconnection networks?

(6+6+6)

5.

a) Explain the functioning of vector processor with the help of suitable diagram?

b) What is Cache Coherence Problem? What is a snooping cache? Discuss with example the Write Through and Write MLE protocols for Cache consistency.

(6+12)

6. Suppose that scalar operations take 10 times longer to execute per result than vector operations. Given a program which is originally written in scalar code:

a) What are the percentage of the code needed to be vectorized in order to achieve the speedup factor of 2, 4 and 6 respectively?

b) Suppose the program contains 15% of code that cannot be vectorized such as sequential I/O operations. Now repeat **question 6. a)** above for the remaining code to achieve the three speed up factors.

(9+9)

7.

a) What are the software tools used for the development of parallel programming?

b) Define the following:

i) Multilevel page table
ii) Hashing function
iii) Resource conflict
iv) Simple operation latency
v) Address mapping

(8+[5x2])