Code No: R05210504 **Set No. 4**

II B.Tech I Semester Regular Examinations, November 2008
DIGITAL LOGIC DESIGN
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain, How error occurred in a data transmission can be detected using parity bit. [6]
   (b) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend. [5×2]
      i. 111011 - 111000
      ii. 1110-110110
      iii. 10010-1101
      iv. 110-10100
      v. 11011-10000.

2. (a) Reduce the following Boolean expressions.
      i. (AB' + AC')(BC + BC')(ABC)
      ii. AB'C + A'BC + ABC
      iii. (ABC)'(A + B + C)'
      iv. A + B'C (A + (B'C)')
   (b) Obtain the Dual of the following Boolean expressions. [8+8]
      i. ABC + A'B + ABC'
      ii. (BC' + A'D)(AB' + CD')
      iii. x'yz + xz
      iv. xy + x (wz + wz').

3. (a) If F_1= Π 3,4,7,8,11,14,15 and F_2= Σ1,2,4,5,7,8,10,11,12,15 obtain minimal SOP expression for $\overline{F_1 \bullet F_2}$ and draw the circuit using NAND gates.
   (b) Draw the two -level NAND circuit for the following Boolean - expression: $\left(A\overline{B} + C\overline{D}\right) E + BC\,(A + B)$ also obtain minimal SOP expression and draw the circuit using NAND gates. [8+8]

4. (a) Implement 64 × 1 multiplexer with four 16 × 1 and one 4 ×1 multiplexer. (Use only block diagram).
   (b) A combinational logic circuit is defined by the following Boolean functions.
   $F_1 = \overline{ABC} + AC$
   $F_2 = A\overline{BC} + \overline{A}B$
   $F_3 = A\overline{B}C + AB$
   Design the circuit with a decoder and external gates. [8+8]

5. Convert the following:
   (a) J-K flip-flop to T- flip-flop
   (b) R-S flip-flop to J-K-flip-flop
   (c) J-K flip-flop to D- flip-flop
   (d) R-S flip-flop to D-flip-flop. [4+4+4+4]

6. (a) Explain synchronous and ripple counters. Compare their merits and demerits.
   (b) Design a modulo -12 up synchronous counter using T- flip flops and draw the circuit diagram. [8+8]

7. (a) Explain the block diagram of a memory unit. Explain the read and write operation a RAM can perform.
   (b) i. How many 32K * 8 RAM chips are needed to provide a memory capacity of 256K bytes.
   ii. How many lines of the address must be used to access 256K bytes? How many of these lines are connected to the address inputs of all chips?
   iii. How many lines must be decoded for the chip select inputs? Specify the size of the decoder. [8+8]

8. Reduce the number of states in the state table listed below. Use an implication table. [16]

Present state	Next state		Output	
	x=0	x=1	x=0	x=1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	0	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

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