## B. Tech. Degree V Semester Examination, November 2008

## EC/EI 505 MICRO ELECTRONICS & INTEGRATED CIRCUITS (2006 Scheme)

Time:	3 Hours	Maximum Marks:	100
		PART A	
		(Answer ALL questions)	5 - 40)
Ī	a)	Define the term virtual ground in an op amp. How is it different from ordinary ground.	5 = 40)
ı	b)	Draw the circuit of a half wave rectifier using op amp and explain its working with relevant wave forms.	
	c)	Define the term slew rate. Also derive the expression for slew rate in an op amp.	
	d)	Design a first order LPF with a cutoff frequency of 1 KHz and pass band gain of 2.	
	e)	Define the terms a) lock-in-range	
		b) capture range	
	Ð	c) pull-in-time	
	f) g)	How can a PLL be used as a frequency translator.  List 3 advantages and two applications of thick film hybrid ICs.	
	h)	Differentiate between thick film and thin film hybrid ICs.	
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		PART B	
		· ·	4 = 60)
H		For a voltage series feed back amplifier, calculate the closed loop gain, input	
		resistance with feed back, output resistance with feedback and bandwidth with feedback.	(15)
III	a)	OR Define the following op amp characteristics.	
111	a)	i) Input offset voltage	
		ii CMRR	
		iii) SVRR	(6)
	b)	Derive the expression for the output voltage of an op amp integrator. Also calculate	
		the gain limiting frequency.	(9)
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IV		Define the term comparator chatter. How does Schmitt trigger avoid chatter? Explain the working of an inverting Schmitt trigger with necessary waveforms and voltage	
		transfer curve.	(15)
		OR	(15/)
V	a)	Derive the expression for the frequency response of a 2 <sup>nd</sup> order low pass Butterworth filter.	(10)
	b)	Design a 2 <sup>nd</sup> order Butterworth filter having a cut-off frequency of 1KHz.	(5)
VI		Draw the block diagram of a 565 PLL, and explain the functions of major blocks. Also	(15)
		derive the expression for lock-in-range and capture range.	(15)
VII	a)	OR Explain the operation of an R-2R ladder DAC with necessary circuit diagrams.	(6)
V 11	b)	Draw the functional diagram of a monostable multivibrator using timer IC and explain	(0)
	٠,	its operation.	(9)
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VIII	a)	Explain the rules for thin film resistor and capacitor design.	(10)
	b)	Distinguish between i) Monolithic and hybrid ICs.	. = \
		ii) Analog and Digital IC	(5)
lX	e)	OR Explain the two basic processes in thick film processing.	(10)
ιΛ	a) b)	What are the major steps in the design guidelines for thick film hybrid ICs	(5)
	٠,	And the major steps in the seeds Barachines for their initiation to	(2)
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