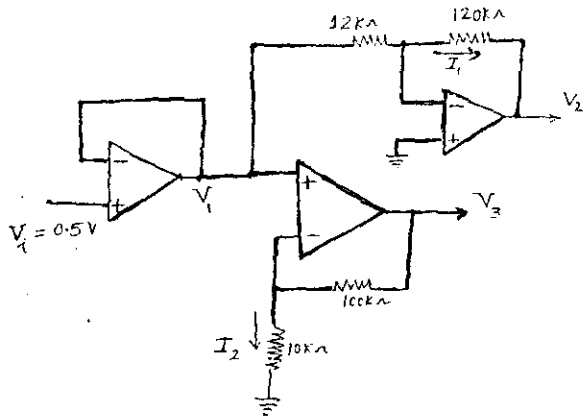
MODULE - V

IX a) Explain the Basic principles of a Difference Amplifier & distinguish between
(i) Common signal Mode of operation &
(ii) Differential signal mode of operation.
Define CMRR. (10)

b) Identify each Op-Amp stage & calculate the output voltages V_1, V_2 & V_3. Calculate the currents I_1 & I_2 (10)

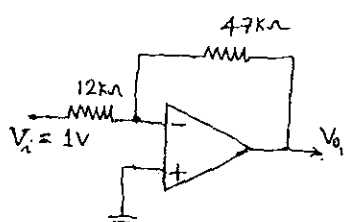


OR

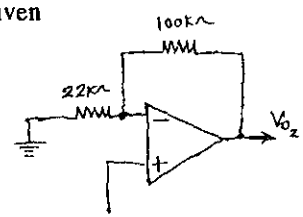
X a) Draw a schematic diagram of an Integrated circuit Op-Amp system & explain the function & important charactersitics of each stage. (8)

b) Compare the following charactersitics of an Ideal Op-Amp with those of Real (practical Op-Amp by giving typical values.
(i) output offset voltage, (ii) Input Bias currents
(iii) Open loop voltage gain. (6)

c) Determine the closed loop voltage gains & the input resistance of the Op-Amp circuits given (6)



A_{vf} =
R_{in} =
Vo_1 =



A_{vf} =
R_{in} =
Vo_2 =

Calculate Vo_1 & Vo_2.

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Code No. BTS 005(C)

B.Tech. Degree III Semester Examination in Computer Science and Engineering, January 2001

CS 305 ELECTRONIC CIRCUITS

Time: 3 Hours *Max. Marks: 100*

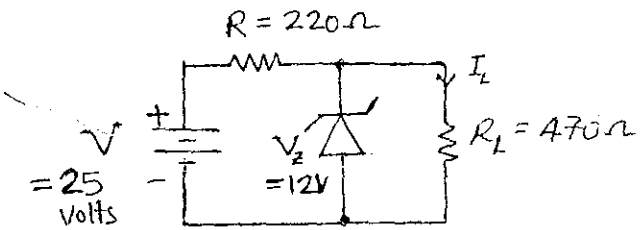
Instructions: 1) Answer 5 questions choosing one question from each Module.
2) Each question carries 20 marks
3) Draw neat sketches, circuit diagrams, where they are required.

MODULE - I

I a) Sketch the input and output charactersitics of an NPN silicon Transistor & indicate the different regions of operation on the characteristics. Draw a suitable circuit which may be used to obtain the input & output characteristics of an NPN transistor in CE configuration. Write equations for the input current, output current and collecter - emitter voltage, in the circuit that you have drawn. (10)

b) Calculate the output collector current & I_{CEO} for an NPN transistor in CE configuration if $I_B = 50\ \mu A$, $\beta = 80$, $I_{CBO} = 200nA$. (5)

c) In the circuit shown calculate I_R, I_L & I_Z. Calculate the maximum power dissipation in the zener diode. (5)



OR

II a) Explain the following with reference to JFET. (i) Pinch - off voltage, (ii) I_{DSS}, (iii) Gate - source cut off voltage (iv) Transconductance. (10)

b) Draw an UJT circuit which can be used to obtain the Emitter characteristics. Draw a set of Emitter characteristics of an UJT & indicate all the salient features. (5)

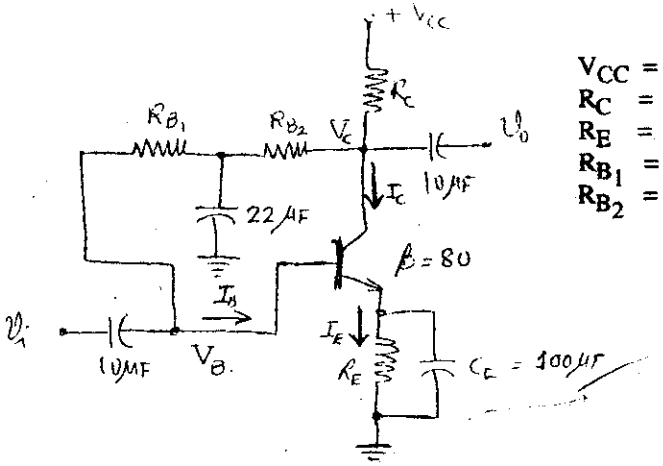
(P.T.O)

c) Write the "Shockley's equation" for the drain current of a JFET. Calculate I_D. If I_{DSS} = 10mA, & V_p = 4 Volts at V_{as} = – 1V (5)

MODULE - II

III a) Draw the following Transistor Biassing circuits & write equations to show the calculations of DC Quiescent state currents & voltages.
(i) Fixed Bias Circuit
(ii) Collector to Base Biassing Circuit. (10)

b) Calculate I_B, I_C, I_E, V_B, V_E, V_C & V_{CE} for the Transistor circuit shown. Assume the Transistor to be silicon. In what region does the Trnasistor operate? (10)



V_{CC} = 15 Volts
R_C = 3.3 KΩ
R_E = 470 Ω
R_{B_1} = 100KΩ
R_{B_2} = 120KΩ

OR

IV a) Sketch an RC coupled Amplifier circuit which is operated in the CE configuration & explain how this circuit operates as an amplifier. Draw the input base signal, collector current & collector voltage waveform. Indicate how you can draw the load line (DC') for the circuit you have drawn. (10)

b) Draw a common Emitter Amplifier circuit using a voltage divider type of Biass - using the approximate h-parameter equivalent circuit. Derive expressions for R_{in}, A_v, A_i & R_o (10)

MODULE - III

V a) What are the advantages of Negative Feed back ?
With schematic diagrams illustrate the different types of Feed back mechanisms employed in amplifier circuits. (10)

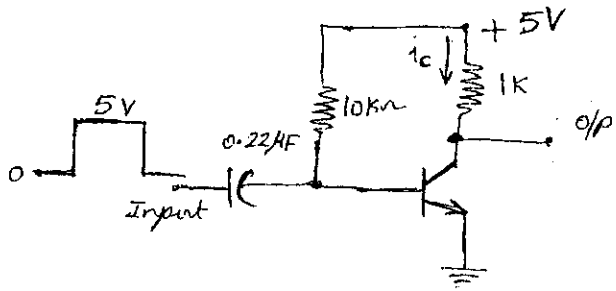
Contd....3

b) With suitable circuit diagrams, bring out the important differences between
(i) Differentiating & Integrating circuits.
(ii) Clipping & clamping circuits. (10)

OR

VI a) With a neat sketch illustrate & explain the following pulse characteristics
(i) Rise time (ii) Over shoot (iii) Ringing, (iv) Fall time & (v) under short. (10)

b) Explain how an NPN silicon Transistor may be used as a switch.
In the circuit shown, calculate the Maximum collector current, Maximum & Minimum collector voltages, when the input pulse is applied. Assume $V_{BE(sat)}$ = 0.7 V $V_{CE(sat)}$ = 0.1V. Sketch the collector current & collector voltage wave forms assuming the Rise and fall times of i_c as equal to 25% of Input pulse width. (10)



MODULE - IV

VII a) With suitable diagrams, explain the differences between Class-A, Class-B & Class-C types of Power Amplifiers. (10)

b) Draw a complementary symmetry push pull circuit & explain its operation with relevant wave forms. (10)

OR

VIII a) Explain with a neat schematic diagram how a sinusoidal oscillator can be built. Establish the Bark Hausen's criteria, for sustained oscillations, starting from Basic Fundamentals. (10)

b) Calculate the Gain of the amplifier necessary so as to satisfy the Bark Hausen's criteria, if the Feed back used in the system is 5%. (5)

c) Compare the LC oscillators with crystal oscillators. (5)

Contd...4