B.Tech. Degree VI Semester (Supplementary) Examination, October 2009

CS/EC/EI/EE 601 DIGITAL SIGNAL PROCESSING

(1999 Scheme)

Time: 3 Hours Maximum Marks: 100

I. (a) Define
(i) linearity (ii) causality (iii) time invariance of discrete systems (8)

(b) Find the inverse z transform of

$$X(z)=\frac{1+2z^{-1}+z^{-2}}{1-\frac{3}{2}z^{-1}+\frac{1}{2}z^{-2}} \quad x[n] \quad \text{causal} \qquad (12)$$

OR

II. (a) What is system function? What is its significance? (6)

(b) Why can't ideal filters be realized? (4)

(c) Find the inverse z transform of $x[n]$ of $X(z)=\frac{1}{1-az^{-1}}$ by long division, where $x[n]$ is an anticausal sequence. What is its R.D.C? (10)

III. (a) Describe the block convolution method using overlap add and overlap save schemes. (12)

(b) Find the total multiplications and additions (complex as well as real) for computing an N point DFT. What is the computational saving when N is a power of 2 and radix 2 FFT is used. (8)

OR

IV. (a) Show using a numerical example that circular convolution is linear convolution followed by time aliasing. (10)

(b) Draw the signal flow graph for an 8 point Radix – 2 DIT FFT. (10)

V. (a) Show that FIR filters can be designed with constant phase delay and constant group delay. (10)

(b) Discuss the windowing method of FIR filter design. What is Gibb's phenomenon? (10)

OR

VI. (a) Compare IIR and FIR filters. (10)

(b) Discuss the frequency sampling technique for FIR filter design. (10)

VII. (a) Implement the following filter in Direct form I, Direct form II and Cascade (12)

$$H(z)=\frac{1+0.75z^{-1}+0.125z^{-2}}{1-1.75z^{-1}+0.875z^{-2}-0.1251z^{-3}}$$

(b) Discuss the Bilinear transformation method. What is frequency warping. (8)

(Turn Over)

OR

VIII.	(a)	Compare the characteristics of direct form 1, direct form 2, cascade and parallel forms of realizing IIR filters.	(10)
	(b)	Determine the order and poles of a Low pass Butter worth filter that has a 3 dB attenuation at 500 Hz and an attenuation of 40 dB at 1000 Hz.	(10)
IX.	(a)	Draw and explain the block diagram of a typical DSP processor.	(10)
	(b)	What do you mean by limit cycle oscillation. Illustrate with example.	(10)

OR

X.	(a)	Discuss any two DSP applications.	(12)
	(b)	Explain the need for scaling the input signal in saturated arithmetic.	(8)

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