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R 321

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2005.

Fourth Semester

Electronics and Communication Engineering

EC 242 — DIGITAL ELECTRONICS

Time : Three hours Maximum : 100 marks

Answer ALL the questions.

PART A — (10 × 2 = 20 marks)

1. State Demorgan's laws.

2. Simplify $A + AB + \overline{A} + B$.

3. Define noise margin.

4. What are tri–state gates?

5. What is a combinational circuit? Give an example.

6. What is a sequential circuit? Give an example.

7. What is PLA?

8. Draw the logic diagram of SR flip flop.

9. Define cycles.

10. Define a stable state.

PART B — (5 × 16 = 80 marks)

11. (i) Explain races and hazards with suitable examples. (8)

(ii) Discuss methods of designing race free and hazard free circuits with examples. (8)

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12. (a) (i) Minimise the following using Karnaugh map. Implement the resultant function using NOR gates only.

$$f(A, B, C, D, E) = \pi M(2, 4, 7, 9, 26, 28, 29, 31).$$ (12)

(ii) Write notes on computer aided minimisation procedures. (4)

Or

(b) (i) Simplify the following function using tabulation procedure. Implement the reduced function using NAND gates only.

$$f = \sum m(0, 1, 3, 5, 6, 9, 11, 14, 21, 23, 24, 31) + \sum d(25, 30).$$ (12)

(ii) Define maxterms and minterms. Give examples. (4)

13. (a) (i) Explain the working of a TTL NAND gate. (12)

(ii) Write notes on HTL gate. (4)

Or

(b) (i) Explain the working of a CMOS logic gate. (12)

(ii) Write notes on ECL gate. (4)

14. (a) (i) Design and explain the working of full adder and a decoder. (12)

(ii) Write notes on EPROM. (4)

Or

(b) Design and explain the working of a Gray to BCD converter.

15. (a) (i) Explain the working of a master–slave JK flip flop. (8)

(ii) Write notes on memory decoding. (8)

Or

(b) (i) Design and explain the working of a mod–11 counter. (8)

(ii) Explain the techniques of state minimisation using an example. (8)

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