SATHYABAMA UNIVERSITY

(Established under section 3 of UGC Act, 1956)

Course & Branch: B.E - CSE
Title of the paper: VLSI System Fundamentals
Semester: V — Max. Marks: 80
Sub.Code: 411501/511501/611501 — Time: 3 Hours
Date: 06-11-2008 — Session: FN

PART – A (10 x 2 = 20)

Answer All the Questions

1. Write an expression to find threshold voltage of a MOs transistor.

2. Write the truth table for a four-way multiplexer.

3. Draw the diagram of a CMOS inverter.

4. State and briefly explain the secondary effect in a MOSFET.

5. Briefly explain the differences between two types of synchronous state machines.

6. What is meant by aspect ratio of a CMOS device?

7. List the types of adders.

8. State the types of ASIC.

9. What is a pass transistor?

10. What are the advantages of CMOS technology?

PART – B (5 x 12 = 60)

Answer All the Questions

11. (a) Explain the transfer characteristics of a CMOS inverter.
    (b) Explain the operation of n-MOS enchancement transistor.

(or)

12. (a) Explain dynamic power dissipation in a MOSFET.
    (b) Design a Moore's state machine using D-flipflops.

13. (a) Explain CMOS Domino logic circuit and its versions.
    (b) Explain Cascade Voltage Swithch Logic (CVSL)

(or)

14. (a) Give a comparative statement between static and dynamic CMOS design.
    (b) Explain the secondary effects in a MOSFET.

15. Explain a 16 x 16 booth multiplier.

(or)

16. Explain C^2 MOS latch – pipelining.

17. Describe Kernighan Lin partitioning algorithm.

(or)

18. Describe simulated annealing in partitioning.

19. Explain the following:
    (a) Goals and objectives of floorplanning.
    (b) Measurement of delays during floorplanning.
    (c) Floorplanning tools.

(or)

20. Explain:
    (a) force-directed placement algorithm.
    (b) Input-Output and power planning.