Register Number | | | | | | | |

SATHYABAMA UNIVERSITY

(Established under section 3 of UGC Act, 1956)

Course & Branch: B.E-CSE
Title of the Paper: VLSI System Fundamentals Max. Marks: 80
Sub. Code: 611501 Time: 3 Hours
Date: 12/11/2010 Session: FN

PART - A (10 X 2 = 20)

Answer ALL the Questions

1. Differentiate Mealy and Moore state machine.

2. Define threshold voltage.

3. What is ratioed logic style?

4. Define electrical effort.

5. Draw the ratioed CMOS latch.

6. Define pipelining.

7. What are the advantage and disadvantages of KL algorithm?

8. What are the goals and objectives of systems portioning?

9. What are the objectives of floor planning?

10. List the factors that are considered during floor planning.

PART – B (5 x 12 = 60)

Answer All the Questions

11. Derive the CMOS voltage relations and threshold voltage.

(or)

12. Design a toll gate control using flipflops.

13. Explain the different design techniques to reduce switching activity.

(or)

14. Design a 4 input NAND gate using dynamic CMOS logic and explain.

15. Explain C^2MOS and TSPCR register with example.

(or)

16. Explain booth multiplier with example.

17. Explain simulated annealing portioning method.

(or)

18. Compare constructive and iterative partitioning. Describe any one iterative improvement algorithm.

19. Explain the clock, power and input output planning in ASIC design.

(or)

20. Explain iterative placement algorithm with suitable example.