Register Number | | | | | | | |

# SATHYABAMA UNIVERSITY

(Established under section 3 of UGC Act,1956)

Course & Branch :B.E - CSE
Title of the Paper :VLSI System Fundamentals Max. Marks :80
Sub. Code :611501 Time : 3 Hours
Date :09/11/2009 Session :FN

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PART - A (10 x 2 = 20)

Answer ALL the Questions

1. Define MOs transistor.

2. Draw CMOS inverter.

3. What are the advantages of Pass transistor?

4. What is domino logic?

5. Differentiate between static and dynamic sequential circuits.

6. What are the advantages of $C^2$MOs?

7. Differentiate between constructive partitioning and iterative partitioning.

8. What are the disadvantages of KL algorithm?

9. What are the objectives of Floorplanning?

10. Draw the Gajaski's Y Chart.

PART – B (5 x 12 = 60)

Answer All the Questions

11. Derive the current and voltage relations of a MOS transistor.

(or)

12. Explain the working of a CMOs inverter.

13. Explain pass transistor logic.

(or)

14. Explain the dynamic CMOS design.

15. Explain Booth multiplier with example.

(or)

16. Write short notes on:
    (a) $C^2$MOS Latch
    (b) Latch Pipelining

17. Explain Kernighan Lin algorithm.

(or)

18. What is simulated annealing? How simulated annealing can be applied for partitioning of VLSI circuits?

19. Explain force directed placement algorithm.

(or)

20. What are the different floor planning tools? Explain how it is used for floorplanning.